Serial ATA International Organization

Serial ATA Interoperability Program Revision 1.6
Unified Test Document (UTD) Version 1.1

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Serial ATA International Organization, Serial ATA Interoperability Program Unified Test Document is available for download at http://www.sata-io.org.

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All test procedures and techniques outlined in this UTD shall be free of restriction necessary for implementation and shall observe absolute IP neutrality. Should a member identify any section of this document which references or suggests test methodology which is restricted, it should be brought to the attention to the Logo committee and reviewed with the intent of removal from this document.

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Version History

Version	Date	Comments
1.1	11/13/2020	Released

Revision History

Rev 1.1
- PHY/TSG/OOB
  - SATA 2.5 ECN 018 – Updated LBP
- RX/TX
  - SATA 2.5 ECN 021 – Gen 1 Return Loss (RX-06 / TX-06) added
  - SATA 2.5 ECN 023 – Common mode return loss adjusted (RX-04 / TX-04 limits adjusted)
  - SATA 2.5 ECN 024 – NRZ/Idle state requirements (all RX / TX measurements adjusted)
- System Interop – Added ATAPI drive support
- Cable Mechanical – Insertion / removal and pull-out
- Pretest - Added
- Informative tests:
  - RSG and Host Digital

Rev 1.2
- Product Electrical – RSG – 10/33/62 MHz – normative
- Product Electrical – RX/TX – Removed 2ns option for RX-01 / TX-01
- Device Digital –
  - Split Host and Digital IPM apart,
  - GTR-05 informative,
  - Added IPM 10 second time outs
- Device Mechanical – Add Slimline
- Pretest – Changed from 2 ALIGN to 4 ALIGN Framed COMP Pattern
- Informative tests: Host Digital

Rev 1.3
- Changed references from SATA 2.5 to
- Product Electrical – PHY/TSG/OOB
  - SATA 3.0 ECN 008 – JTF Calibration impacted TSG-09 / -10 / -11 / -12
  - SATA 3.0 ECN 016 – Long Term Frequency stability & SSC – impacted PHY-02 / -04
  - SATA 3.0 ECN 017 – OOB – impacted OOB-02 / -03 / -04 / -05, -06 / -07
- Product Electrical – RSG – Added 5 MHz Sj
  - SATA 3.0 ECN 009 – Framed COMP pattern use SATA 2.5 ECN 018 LBP pattern
- Product Electrical – RX/TX – RX-02 / TX-02 obsolete
- Pretest – Changed back to 2 ALIGN Framed COMP Pattern
- Digital – Host – normative
- Digital – Device – Documented minimum loop counts (IPM-03 / -04 / -11)
- Informative tests:
  - Cable - eSATA cable (electrical and mechanical)
  - Product Mechanical - eSATA mechanical
  - Digital - Port Multiplier
  - Device Mechanical - uSATA

Rev 1.4
- Added a list of ECN work items which need to be incorporated into the UTD Rev 1.4.
- TX and RX testing made Informative
- Renamed Framed Comp to FCOMP and removed reference to Long Comp Pattern

Changed references to uSATA to Micro SATA for consistency with main spec.
Clarified ASR-03 measurement requirements
Added measurement requirement to SSP-12
OOB-06 added different measurement requirements for hosts versus devices and clarified number of bursts to be captured
OOB-07 clarified number of bursts to be captured
Removed proposed (and rejected) OOB-08

Rev. 1.5

Added base jitter limit requirement to RSG-06
Added “Alternative sequence” for OOB-06
Added M.2 mechanical references in PCI Express M.2 Specification
Added TSG-17
Added intro statement to OOB-06
Changed OOB-06 host value from 174 to 2 720
Added IPM-12 & IPM-13 as Informative tests
Deleted Section 3.4 (reference to template)
Added SLP-01 to SLP-10

Rev. 1.6

Updated to Serial ATA Revision 3.5
Replaced section 2.1 & 2.2 with reference to base, updated section 1.3 to a table and UTD Impact

Rev. 1.6 Version 1.1

Updated to Serial ATA Revision 3.5
Changed all references from “align timing” to ALIGNp
Changed IPM-01 and IPM-09 host measurements to be from COMWAKE to ALIGNp

Table of Contents

1 Goals, objectives, and constraints

1.1 Overview

This document defines the test requirements specific to the SATA-IO Interoperability Program. Many of the test requirements are associated with a subset of requirements included in Serial ATA Revision 3.5 and these test requirements are based upon the requirements for the Serial ATA protocol and features, intended to verify a subset of the Specification requirements and ensuring compatibility for Serial ATA. Not every feature or capability within the Serial ATA architecture may be included in the Integrator's List testing. The requirements are driven by the necessary capabilities of the Specification that are to be verified by functional testing. There are additional test requirements which are intended to verify general system interoperability which are not associated with any Specification requirements.

Some of the goals and requirements for the Interoperability Program documentation include:

a) maintain adherence to Serial ATA Specification(s) across all SATA products;
b) maintain compatibility with older hosts and devices without compromising product adherence to the Specification; and
c) deliver standard test requirements for Serial ATA products.

1.2 References

This document is not a Serial ATA Specification, but includes requirements for testing adherence to a subset of the Serial ATA Specification guidelines, in addition to system interoperability tests. This document makes reference to the following Specifications and documents:

a) Serial ATA Revision 3.5. Available for download at www.sata-io.org;
b) AT Attachment with Packet Interface – 6 (ATA/ATAPI-6). Draft available at www.t13.org. Published ATA/ATAPI Specifications available from ANSI at webstore.ansi.org or from Global Engineering;
c) ACS-4: INCITS 529-201x ATA Command Set – 4 (ACS-4). Draft available at www.t13.org. Published ATA/ATAPI Specifications available from ANSI at webstore.ansi.org or from Global Engineering;
d) Serial ATA Interoperability Program Revision 1.3 Policy Document. Available for download at www.sata-io.org; and
e) Serial ATA Interoperability Program Revision 1.3 Description Document. Available for download at www.sata-io.org.

1.3 Changes

Change #	Description	UTD Impact
Changes to Serial ATA Revision 2.5		
ECN001	COMWAKE retransmission	No impact
ECN002	Device Configuration Overlay	No impact
ECN003	L_BadEnd and DFPDMAQ8	No impact
ECN004	Table 14 rise times	Included – Impacted TSG-02
ECN005	Cable test methodology	Included – Impacted SI-01 to SI-04
ECN006	L_RdvData and PIO Setup FIS	No impact
ECN007	READ LOG EXT clear SActive	No impact
ECN008	SYNC Escape in PIO-in	No impact
ECN009	Return-loss impedance balance	Included – Impacted TX-05 and RX-05
ECN010	20 Dword latency	No impact
ECN011	ICRC bit in DPIOI3 and DPIOO3	No impact
ECN013	eSATA connector bump	No impact

Change #	Description	UTD Impact
ECN014	OOB timing	Included- Impacted OOB-01 to OOB-07
ECN015	LT6:L_SendHold transition to LT7:L_SendCRC	No impact
ECN018	LBP running disparity fix	Included – Impacted TSG-01, TSG-09 to TSG-13, TSG-15, and RSG setup
ECN019	BIST Activate FIS patterns	No impact
ECN020	Connector bump tolerances	Included – Impacted MCI-01
ECN021	Termination measured TDR or return loss	Included – Impacted TX-01 and TX-02
ECN023	Common mode return loss relaxed	Included – Impacted TX-04 and RX-04
ECN024	Impedance measurements applied signal	Included – Impacted TX-04 and TX-08
Changes to Serial ATA Revision 2.6		
ECN001v0	Slimline Bump Correction	No impact
ECN002v0	Latching Receptacle Bump Correction	No impact
ECN003v1	State Name Corrections	No impact
ECN004v2	Reserved SATA Log Page Numbers	No impact
ECN006v1	Remove F(baud)/10 requirement	Impacted area already informative
ECN008v1	Clarify JTF used for F(baud)/500 measurement	Included – Impacted TSG and RSG tests
ECN009	LBP_COMP description	Included – Impacted RSG tests and System Interop
ECN010v0	IPM Resume Speed	Already included
ECN011v5	Valid data and CRC requirements	No impact
ECN012v0	Correct bump tolerance overlap	No impact
ECN013v2	Editorial correction, IDENTIFY PACKET DEVICE table.	No impact
ECN014v0	PACKETstatenames	No impact
ECN016	LongTermFreqAccuracy_and_SSC_Tests	Included – Impacted tests PHY-02 and PHY-04
ECN017	OOB Burst/Gap Measurement	Included – added clarification to OOB section
ECN018v0	Correct Slimline power connector dimensions	No impact
ECN019v2	Cable ISI Test Source Risetime	Included – Impacted test SI-09
ECN021	Correct internal height dimension for eSATA plug	Included in MXE-01a
ECN022v1	Remove references to “KB”	No impact
ECN023v1	Key Opening Correction (Slimline Host Receptacle Connector)	No impact
ECN024	Impedance measurements	Included – Impacted tests TX-01 to TX-06 and RX-01 to RX-06
ECN025v1	Rise Time Measurements	Included – Impacted TSG-02
ECN027v1	Gen3i Rx Differential Return Loss Text Description and Figure Change – Clarification Only	Included – Impacted TX-07 and RX-07
ECN028	Clarification of Test Patterns for Measurements Defined in 7.2 Electrical Specifications	No impact

Change #	Description	UTD Impact
ECN029	Addition of Pattern to the TX AC Common Mode Voltage (Gen3i) Measurement Description	Included – Impacted TSG-04 and TSG-16
ECN030v1	Grammatical Error in Section 7.3.2.3	No impact
ECN031	Corrections to ECN # 004	No impact
ECN032	Correction to TX AC Common Mode Voltage Table Value 'Units'	Included – Impacted TSG-16
ECN033v2	Definitions of Terms	No impact
ECN034v2	Corrections to Serial ATA Technical Proposal # 005	Included – Impacted DOF-02
ECN035v1	Clarification of Words 76 to 79	No impact
ECN036v31	LIF SATA Clarifications	No impact
ECN037	Technical Integration WG changes	No impact
ECN038	Key clarification	No impact
And the following new features and enhancements		
TPR002	Gen3 register assignments	No impact
TPR004	NCQ clarifications	No impact
TPR005v2	SATA Speed Indicator in ID String	Included – Impacted DOF-02
TPR007v4	Automatic Partial to Slumber Transitions	No impact
TPR009v1	LIF Connector for 1.8" HDD for SATA Revision 2.6	No impact
TPR010v1.1	Serial ATA NCQ Streaming Command	No impact
TPR011v1	Serial ATA NCQ QUEUE MANAGEMENT Command	No impact
TPR012v1	Gen 1 Clock to Data Jitter Definition	Included – Impacted TSG-09
TPR013v1	Connector for 7mm slimline drives	No impact
TPR014v6	Allow READ LOG DMA EXT to Clear NCQ Error	No impact
TPR015	Remove Device Register from Signature	Included – Added keyword na for not applicable and GTR-01
TPR016	Add Write-Read-Verify to SSP support	Included – Impacted SSP-12
TPR017	ATA8 ACS Alignment	No impact
TPR018	6G PHY Working Group Specification Revisions For Gen3i	Included – Added Gen3i
Release that incorporates errata against Revision 3.0		
ECN039	Gen3i TX Jitter Compliance Requirements	Included – Impacted TSG-13
ECN040	DCO Corrections	No impact
ECN041	To correct SATA Internal 4 Lane Pin assignments, Figure 44	No impact
ECN042	mSATA Connector Pin Counts of Vendor Specific and Reserved Pins	No impact
ECN043	Correction to description of ASR	No impact
ECN044	Mathematical CIC for Gen3i	No impact
ECN045	Interface Detect Pin for mSATA Connector and the following new features and enhancements	No impact
ECN046	IDENTIFY DEVICE words 63, 78 and 79	Included – Impacted SSP-13
ECN047	Correction to description of APS status in Identify Packet Device	No impact
ECN048	RX Impedance Balance Correction	Included – Impacted RX-05
ECN049	P51 Pull-Down Resistor Value and Reference Circuit and P43 Definition	No impact

Change #	Description	UTD Impact
ECN050	Asymmetric Amplitude and revisions to Minimum Amplitude measurement methodology	Included – Impacted TSG-15 and RSG calibration
ECN051	Change of receiver test pattern specification to include Logo Framed Composite Pattern	Included – Impacted RSG-05, RSG-06, and SYT-09
ECN052	Clarification of the Gen3i RX Tolerance Test Signal Amplitude Calibration Methodology	Included – Impacted RSG-03 and RSG calibration
ECN053	Gen-III (6Gbps) RiseTime Specification Change	Included – Impacted TSG-02
ECN054	Change to EMI Related Parameters: TX Rise/Fall Imbalance - Elimination, and TX Amplitude Imbalance - Margin Increase	Included – Impacted TSG-05 and TGS-06
ECN055	Consistency of Register FIS nomenclature	No impact
And the following new features and enhancements		
TPR003	SSC Profile df/dt Excursion Limitation	No impact
TPR019	HOLDP/HOLDAP Protocol Change for 6G SATA	No impact
TPR020	Extensions to the FPDMA QUEUED Command Protocol to Support Fixed 512 Byte Block Transfer DMA Commands	No impact
TPR021	Speed Clarification	Included – Impacted GTR-02
TPR022	Required Link Power Management	Included – Impacted IPM-12
TPR023	Apply SATA 2.5 Design Guide 2 for all devices	No impact
TPR024	mSATA Connector	Included – Impacted MDI-01
TPR025	NCQ Status bit 4	No impact
TPR026	Zero Power Slimline ODD	No impact
TPR027	Add Sanitize State to SSP support	No impact
TPR028	Micro SATA Connector P7 Definition	No impact
TPR029	Clarification of Speed Negotiation	No impact
TPR030	Gen1x, Gen2x Removal	No impact
TPR031	Hardware Control Feature Mechanism	No impact
TPR032	COMINIT after POR Timing	Included – Impacted ASR-01
TPR034	SATA Universal Storage Module	No impact
TPR036	NCQ Autosense	No impact
Release that incorporates errata against Revision 3.1		
ECN056	Tx AC Common Mode Voltage Change for Gen3	Impacted TSG-16
ECN057	Internal Micro SATA and Slimline Gen3	No impact
ECN058	Hardware Feature Control Correction	No impact
ECN059	Device Configuration Overlay Correction	No impact
ECN061	Dual Consecutive ALIGNp Sequence	No impact
ECN062	Tx Min Amplitude Cleanup	Included – Impacted TSG-15
ECN063	Rx Rise/Fall Time Reinstated	Included – Impacted RSG calibration
ECN064	ErrorFlush Cleanup	No impact
ECN065	Identify Modification	Included – Impacted SSP-13
ECN066	Tx AC Common Mode Voltage Procedural Simplification	Impacted TSG-16
ECN067	Port Multiplier Signature for Software Reset, Description of I field of Set Device Bits FIS, NCQ Queue Management Subcommand response, Typo Error in GSCR Reference	No impact
ECN068	Device Sleep Voltage Spec Adjustment	No impact
ECN069	Hardware Feature Control Bug	No impact

Change #	Description	UTD Impact
ECN070	PM5:PUIS Clarification	No impact
ECN071	DEVSLP Bit Interlock	Included – Impacted SLP-01
ECN072	Endianness of LBA Range List	No impact
And the following new features and enhancements		
TPR033	Relaxation of Minimum Transmit Rise/Fall Times for Gen 1 and Gen 2	Included – Impacted TSG-02
TPR035	SATA BGA SSD	No impact
TPR037	Standard SATA Connector 3.3V Power Pin Assignments	No impact
TPR038	Device Sleep	Included – Added section 3.7 and SPL-01 to SPL-10
TPR039	DEVSLP Assignment on Standard SATA Connector	No impact
TPR040	Software Settings Preservation for Device Initiated Interface Power Management	Included – Impacted SSP-13
TPR041	9 mm SATA USM	No impact
TPR042	Hybrid Information Feature	No impact
TPR043	Queuing Power Management	No impact
TPR044	Synch with ACS-3	No impact
TPR045	Rebuild Assist	No impact
TPR046	Transitional Energy Reporting	No impact
TPR047	SATA Express Specification	No impact
TPR049	Add QPM to SATA logs	No impact
TPR050	SATA MicroSSD Footprint Update	No impact
TPR051	Hybrid Information Update	No impact
TPR053	M.2 Card Formfactor for SSDs	Included – Impacted MDI-01
TPR054	SATA 8.5 mm Slimline ODD Connector Location	No impact
Release that incorporates errata against Revision 3.2		
ECN073	CIC Clarification	No impact
ECN074	SATA Express Pin Sequencing	No impact
ECN075	Identify Device data log and Word correction	No impact
ECN076	Flow control	No impact
ECN077	Automatic Partial to Slumber No NCQ	No impact
ECN078	Queued Error I-bit Correction	No impact
ECN079	TPR056 Corrections for Power Disable	Included – Impacted SLP-05
ECN080	NCQ Feature Set Clarification	No impact
ECN081	Missing bit in ID data log for Rebuild Assist	No impact
ECN082	FCOMP D24.2 Correction;	Included – Impacted 5.6
ECN083	Tx impedance balance cleanup	Included – Impacted TX-05
ECN084	Slimline Figure Move	No impact
ECN085	mSATA Figure Cleanup	No impact
ECN086	Clarifying NCQ Commands	No impact
ECN087	Missing bit in ID data log for Hybrid Information Enable	No impact
ECN088	Enclosure services signature	No impact
ECN089	DAS/DSS Support Clarifications	No impact
And the following new features and enhancements		
TPR056	Enable new Power Disable feature on standard SATA connector P3	No impact

Change #	Description	UTD Impact
TPR057	Register Signature definition for Host Managed Zoned devices	No impact
TPR058	DAS/DSS/DHU Changes	No impact
TPR059	Emphasis Control for SATA Interface	Included- Impacted TSG-17
TPR060	Modify/Cleanup Receive FPDMA Queued to support ZAC	No impact
TPR061	Define/Use Sequential NCQ command(s)	No impact
TPR062	SEND/RECEIVE FPDMA Queued Cleanup	No impact
TPR063	Align Queued DATA SET MANAGEMENT with ACS-4	No impact
TPR064	Queued version of ACS-4 ZERO EXT command	No impact
TPR065	Modernize Aux Field in NCQ NON-DATA Command	No impact
TPR066	Reporting Current Write Pointer for NCQ Errors in Write Pointer Zones	No impact
TPR067	FPDMA Zone Management Commands	No impact
TPR068	Clarification of the FPDMA state machine and error reporting	No impact
TPR069	MFTP Measurement Method for Emphasis	Included – Impacted TSG-17
TPR070	Retire ICC Field in SEND / RECEIVE FPDMA QUEUED	No impact
TPR071	Addition of ZAC Management In/Out to NCQ Non-Data log (12h) and NCQ Send and Receive log (13h)	No impact
TPR072	Add Deferred Errors to NCQ Error log	No impact
TPR073	IDENTIFY DEVICE Revision Updates	No impact
TPR074	Obsolete Parallel ATA Emulation	No impact
TPR075	Add DATA SET MANAGEMENT XL command	No impact
Release that incorporates errata against Revision 3.3		
ECN090	Correction of reference to SRST	No impact
ECN091	Correction to Power Disable	No impact
ECN092	Support Cache Behavior Bit Clarification	No impact
ECN093	DIPM and HIPM Corrections	No impact
ECN094	Phy Event Counters Log Fix	No impact
And the following new features and enhancements		
TPR076	Durable/Ordered Write Notification	No impact
TPR077	DEADLINE HANDLING Correction	No impact
TPR078	Clarification on writeable logs	No impact
TPR079	Correction of references to tagged command queueing	No impact
TPR080	Additional DevSlp timing requirement	Included – Impacted SLP-06, SLP-07, SLP-09, and SLP-10
TPR081	Out of band management control structures	No impact
TPR082	Obsolete SATA Express	No impact

2 Definitions, abbreviations, and conventions

2.1 Terminology

2.1.1 Definitions and abbreviations

For definitions and abbreviations see Serial ATA Revision 3.5 specification.

2.2 Conventions

For conventions see Serial ATA Revision 3.5 specification.

2.3 Product classes

2.3.1 Test requirements

Due to the difference in architecture and design of Serial ATA products, the test requirements shall be distinguishable between the following types of products:

a) Device:
   A) hard disk drive;
   B) hybrid;
   C) half-height ATAPI device;
   D) slimline ATAPI device;
   E) eSATA device; or
   F) SATA MicroSSD;
b) Cable:
   A) standard internal;
   B) LIF;
   C) multi lane; or
   D) eSATA;
c) Host:
   A) HBA;
   B) chipset;
   C) add-in controller; or
   D) eSATA;

or

d) Port Multiplier:
   A) internal; or
   B) eSATA.

Each test associated with a Specification requirement may have separately defined expected behavior for each of the above product classes. In each case, there may be different methodology for both testing the test requirement and determining the pass/fail criteria. Each test requirement shall include the following:

a) expected behavior;
b) measurement requirements; and
c) pass/fail criteria.

The general definition of these subjects is below.

2.3.2 Expected behavior

All of the test requirements have expected behavior as defined in Serial ATA Revision 3.5. All of the expected behavior for each test requirement directly shall refer to the appropriate Serial ATA Specification requirement(s) being tested.

2.3.3 Measurement requirements

Each test requirement contains detailed information necessary for developing tests for verification of the referenced Serial ATA requirement. This information has a possibility of including:

a) types of equipment;
b) testing methodologies;
c) test setup routines; and
d) other helpful information.

2.3.4 Pass/Fail criteria

The pass/fail criteria defined shall be clear and concise, and include specific information necessary to determine passing or failing of a test. Actual results gathered during testing shall be documented in addition to determination of pass vs. fail for a test.

2.4 Methods of implementation

A Method of Implementation (MOI) is defined as documentation specifying test tool details and procedures for the specific use of verifying the different Interoperability test areas. In the future a template for development of a MOI for a specific test tool may be developed, but at this time a MOI, at a minimum, shall include the following:

a) hardware equipment model number(s);
b) software revision number(s);
c) hardware dependencies (e.g., test fixtures);
d) product dependencies (e.g., BIST modes, patterns);
e) detailed procedures for using the equipment to verify the specific Interop test requirements;
f) procedures for extraction of results; and
g) approximate execution time of specific Interop test requirements.

There are different MOI classes which are specific to the different test areas included in this Unified Test Document. Any test tool approved for use in Interoperability Testing shall fall under test execution within one of the following MOI classes:

a) digital/protocol (device/host or port multiplier only);
b) phy electrical (device/host only);
c) phy Tx/Rx requirements (device/host only);
d) RSG requirements (device/host or eSATA only);
e) receiver jitter tolerance (device/host only);
f) mechanical (device/host or eSATA only);
g) cable mechanical (internal or eSATA cable only);
h) cable electrical (internal or eSATA cable only); and
i) system interoperability (device/host only).

It is feasible that separate MOIs are developed for each type of equipment used depending on the class of testing, or that a single MOI is used to cover an entire test class including the details for several pieces of test tool equipment. This shall be determined by the appropriate test tool vendors with considerations from the SATA-IO.

2.5 Test product considerations

2.5.1 Common host/device/Port multiplier BIST considerations

For many of the Phy electrical tests, it is required that a product (Host/Device/Port Multiplier and eSATA versions of these) is able to transmit or loop back patterns which are identified within the Serial ATA Revision 3.5 or this document. There are standard ways of doing this through the BIST protocol per definition within the Specification. If a product does not specifically support either BIST T, A, S, and/or BIST L capabilities, then the vendor needs to bring all equipment to support vendor unique methods for completely emulating BIST T, A, S, and BIST L. This vendor unique process is unable to have substantial impact to the test during interoperability testing (e.g., significant growth in test execution time or complexity of equipment calibration/setup).

2.5.2 Device specific considerations

A device vendor is required to supply at least three samples. In some cases up to two samples maybe run through testing in parallel at a given time. The third sample should be available for backup in case of unexpected errors or failures.

2.5.3 Cable considerations

If a cable assembly product family consists of cables which differ only in their length (e.g., the connector design, cable construction, and assembly method is identical) and if the shortest and longest lengths pass the test requirements, then all intermediate lengths are considered to be passing.

A cable vendor is required to supply at least two identical samples of each length tested.

2.5.4 Host considerations

A host vendor is required to supply at least two samples. In some cases up to two samples may be run through testing in parallel at a given time. In most cases, the second or third sample shall not be secured within a chassis or platform case, as this sample may be used specifically for mechanical testing.

Prior to execution of any testing on a host, a "worst port" for each port type (i.e., internal SATA and/or eSATA) shall be identified. The intent of identifying a worst port is not to validate each port to the Specification, but to simply identify the worst port based on a single relative measurement across all ports within a host. The Interoperability Tests shall then, at a minimum, be processed on the worst port identified per the following procedure:

1) power-on host and ensure test ports are enabled and functional;
2) run the following on each individual port:
    1) connect device;
    2) complete OOB sequence; and
    3) process and record results for the typical Total Jitter (TJ) measurement using the Lone Bit Pattern (LBP) while the host is in NRZ idle following OOB;

and

3) the "worst port" is identified as that which has the highest TJ value recorded on the measurement above.

Relative to the Interface Power Management tests (see 3.5), it is expected that the host product manufacturer supply a facility (i.e., software, or hardware automation) which shall initiate power management state requests in order to support host-initiated test execution – this is only required if the host product claims support for the host-initiated power management capability.

2.5.5 Port multiplier considerations

A port multiplier vendor is required to supply at least two samples. In some cases up to two samples may be run through testing at a given time. In most cases, the second or third sample shall not be secured within a chassis or platform case, as this sample may be used specifically for mechanical testing.

Prior to running any testing on a port multiplier, a "worst port" shall be identified. The intent of identifying a worst port is not to validate each port to the Specification, but to simply identify the worst port based on a single relative measurement across all ports within a port multiplier. The interoperability tests shall, at a minimum, then be processed on the worst port identified per this procedure:

1) power-on port multiplier and ensure test ports are enabled & functional. Run the following on each individual port:
    1) if it is a device port, connect a device and complete OOB sequence;
    2) if it is a host port, connect a host and complete OOB sequence; and
    3) run the test and record results for the typical TJ measurement using LBP while the port multiplier port is in NRZ idle following OOB;

and

2) the worst port is identified as that which has the highest TJ value recorded on the measurement above.

Relative to the Interface Power Management tests (see 3.20.6), it is expected that the port multiplier product manufacturer supply a facility (software, or hardware automation) which shall initiate power management state requests in order to support port multiplier -initiated test execution – this is only required if the host product claims support for the port multiplier -initiated power management capability.

3 Interoperability specification test summary

Table 1 outlines the test requirements for the different types of Serial ATA units under test.

Table 1 - Test Requirements by Product Class

Test GRP	Sec #	Test Req.	Area	Device /Micro SATA HDD	Device ATAPI	Internal Cable Signal	Internal Cable Power	Host	Port Multi-plier *	eSATA Cable*	eSATA host/ device*
GTR	3.1	GTR-01	Digital	M	M	-	-	-	M	-	I
		GTR-02	Digital	F	F	-	-	-	F	-	I
		GTR-03	Digital	M	M	-	-	-	M	-	I
		GTR-04	Digital	M	M	-	-	-	M	-	I
		GTR-05	Digital	*	*	-	-	-	*	-	I
NCQ	3.2	NCQ-01	Digital	F	-	-	-	-	F	-	I
		NCQ-02	Digital	F	-	-	-	-	F	-	I
		NCQ-03	Digital	F	-	-	-	-	F	-	I
		NCQ-04	Digital	F	-	-	-	-	F	-	I
		NCQ-05	Digital	F	-	-	-	-	F	-	I
ASR	3.3	ASR-01	Digital	M	M	-	-	-	M	-	I
		ASR-02	Digital	F	F	-	-	-	F	-	I
		ASR-03	Digital	-	-	-	-	F	-	-	F/-
SSP	3.4	SSP-01	Digital	F	-	-	-	-	F	-	I
		SSP-02	Digital	F	-	-	-	-	F	-	I
		SSP-03	Digital	F	F	-	-	-	F	-	I
		SSP-04	Digital	F	-	-	-	-	F	-	I
		SSP-05	Digital	F	F	-	-	-	F	-	I
		SSP-06	Digital	F	F	-	-	-	F	-	I
		SSP-07	Digital	F	-	-	-	-	F	-	I
		SSP-08	Digital	F	F	-	-	-	F	-	I
		SSP-09	Digital	F	F	-	-	-	F	-	I
		SSP-10	Digital	F	F	-	-	-	F	-	I
		SSP-11	Digital	F	-	-	-	-	F	-	I
		SSP-12	Digital	F	-	-	-	-	F	-	I
		SSP-13	Digital	F	-	-	-	-	F	-	I
		SSP-14	Digital	F	-	-	-	-	F	-	I
IPM	3.5	IPM-01	Digital	F	F	-	-	F	-	-	I
		IPM-02	Digital	F	F	-	-	F	-	-	I
		IPM-03	Digital	F	F	-	-	F	-	-	I
		IPM-04	Digital	F	F	-	-	F	-	-	I
		IPM-05	Digital	F	F	-	-	F	-	-	I
		IPM-06	Digital	F	F	-	-	F	-	-	I
		IPM-07	Digital	F	F	-	-	-	-	-	I
		IPM-08	Digital	F	F	-	-	-	-	-	I
		IPM-09	Digital	F	F	-	-	F	-	-	I
		IPM-10	Digital	F	F	-	-	F	-	-	I
		IPM-11	Digital	F	F	-	-	F	-	-	I
		IPM-12	Digital	F	F	-	-	F	-	-	I
DOF	3.6	DOF-01	Digital	-	F	-	-	-	-	-	I
		DOF-02	Digital	F	F	-	-	-	-	-	I
SLP	3.7	SLP-01	Digital	F	F	-	-	-	-	-	I
		SLP-02	Digital	F	F	-	-	-	-	-	I
		SLP-03	Digital	F	F	-	-	-	-	-	I
		SLP-04	Digital	F	F	-	-	-	-	-	I
		SLP-05	Digital	F	F	-	-	-	-	-	I
		SLP-06	Digital	F	F	-	-	-	-	-	I
		SLP-07	Digital	F	F	-	-	-	-	-	I

Table 1 - Test Requirements by Product Class

Test GRP	Sec #	Test Req.	Area	Device /Micro SATA HDD	Device ATAPI	Internal Cable Signal	Internal Cable Power	Host	Port Multi-plier *	eSATA Cable*	eSATA host/ device*
		SLP-08	Digital	F	F	-	-	-	-	-	I
		SLP-09	Digital	F	F	-	-	F	-	-	I
		SLP-10	Digital	-	-	-	-	F	-	-	I
MCI	3.8	MCI-01	Cable	-	-	M	-	-	-	-	-
		MCI-02	Cable	-	-	M	-	-	-	-	-
		MCI-03	Cable	-	-	F	-	-	-	-	-
		MCI-04	Cable	-	-	F	-	-	-	-	-
MCX		MCX-05	Cable	-	-	M	-	-	-	I	-
MCE		MCE-01	Cable	-	-	-	-	-	-	M	-
SI	3.8.7	SI-01	Cable	-	-	M	-	-	-	I	-
		SI-02	Cable	-	-	M	-	-	-	I	-
		SI-03	Cable	-	-	M	-	-	-	I	-
		SI-04	Cable	-	-	M	-	-	-	I	-
		SI-05	Cable	-	-	M	-	-	-	I-n	-
		SI-06	Cable	-	-	M	-	-	-	I-n	-
		SI-07	Cable	-	-	M	-	-	-	I-n	-
		SI-08	Cable	-	-	M	-	-	-	I	-
		SI-09	Cable	-	-	M	-	-	-	I	-
MDI	3.10	MDI-01	Mech	M	M	-	-	-	-	-	-
		MDI-02	Mech	M	M	-	-	-	-	-	-
MDP	3.11	MDP-01	Mech	M	M	-	-	-	-	-	-
MHI	3.12	MHI-01	Mech	-	-	-	-	*	-	-	-/*
MXE*	3.13	MXE-01	Mech	-	-	-	-	-	-	-	M/M
PHY	3.14	PHY-01	Phy	M	M	-	-	M	F	-	I
		PHY-02	Phy	M	M	-	-	M	F	-	I
		PHY-03	Phy	F	F	-	-	F	F	-	I
		PHY-04	Phy	F	F	-	-	F	F	-	I
TX*	3.15	TX-01	RX/TX	M	M	-	-	M	M	-	I
		TX-02	RX/TX	*	*	-	-	*	*	-	I
		TX-03	RX/TX	F	F	-	-	F	F-n	-	I-n
		TX-04	RX/TX	F	F	-	-	F	F	-	I
		TX-05	RX/TX	F	F	-	-	F	F-n	-	I-n
		TX-06	RX/TX	M	M	-	-	M	M	-	I
		TX-07	RX/TX	M	M	-	-	M	M	-	I
		TX-08	RX/TX	M	M	-	-	M	M	-	I
TSG	3.16	TSG-01	RX/TX	M	M	-	-	M	M	-	I
		TSG-02	Phy	M	M	-	-	M	M	-	I
		TSG-03	Phy	M	M	-	-	M	M	-	I
		TSG-04	Phy	F	F	-	-	F	F	-	I
		TSG-05	Phy	F	F	-	-	F	F	-	I
		TSG-06	Phy	F	F	-	-	F	F	-	I
		TSG-07	Phy	*	*	-	-	*	*	-	I
		TSG-08	Phy	*	*	-	-	*	*	-	I
		TSG-09	Phy	M	M	-	-	M	M	-	I
		TSG-10	Phy	M	M	-	-	M	M	-	I
		TSG-11	Phy	F	F	-	-	F	M	-	I
		TSG-12	Phy	F	F	-	-	F	M	-	I
		TSG-13	Phy	F	F	-	-	F	F	-	-
		TSG-14	Phy	F	F	-	-	F	F	-	-
		TSG-15	Phy	F	F	-	-	F	F	-	-
		TSG-16	Phy	F	F	-	-	F	F	-	-
		TSG-17	Phy	F	F	-	-	F	F	-	-

Table 1 - Test Requirements by Product Class

Test GRP	Sec #	Test Req.	Area	Device /Micro SATA HDD	Device ATAPI	Internal Cable Signal	Internal Cable Power	Host	Port Multi-plier *	eSATA Cable*	eSATA host/ device*
RX*	3.17	RX-01	RX/TX	M	M	-	-	M	M	-	I
		RX-02	RX/TX	*	*	-	-	*	*	-	I
		RX-03	RX/TX	F	F	-	-	F	F-n	-	I-n
		RX-04	RX/TX	F	F	-	-	F	F	-	I
		RX-05	RX/TX	F	F	-	-	F	F-n	-	I-n
		RX-06	RX/TX	M	M	-	-	M	M	-	I
		RX-07	RX/TX	F	F	-	-	F	F	-	I
		RX-08	RX/TX	F	F	-	-	F	F	-	I
RSG	3.18	RSG-01	RSG	M	M	-	-	M	M-n	-	I-n
		RSG-02	RSG	M	M	-	-	M	M-n	-	I-n
		RSG-03	RSG	M	M	-	-	M	M-n	-	I-n
	RFU	RSG-04	RSG								
		RSG-05	RSG	M	M	-	-	M	M-n	-	I-n
		RSG-06	RSG	M	M	-	-	M	M-n	-	I-n
OOB	3.19	OOB-01	Phy	M	M	-	-	M		-	I
		OOB-02	Phy	M	M	-	-	M	M	-	I
		OOB-03	Phy	M	M	-	-	M	M	-	I
		OOB-04	Phy	M	M	-	-	M	M	-	I
		OOB-05	Phy	M	M	-	-	M	M	-	I
		OOB-06	Phy	M	M	-	-	M	M	-	I
		OOB-07	Phy	M	M	-	-	M	M	-	I
PM*	3.20	PM-01	PM	-	-	-	-	-	M	-	F/F
		PM-02	PM	-	-	-	-	-	M	-	F/F
		PM-03	PM	-	-	-	-	-	M	-	F/F
		PM-04	PM	-	-	-	-	-	M	-	F/F
		PM-05	PM	-	-	-	-	-	M	-	F/F
		PM-06	PM	-	-	-	-	-	M	-	F/F
		PM-07	PM	-	-	-	-	-	M	-	F/F
		PM-08	PM	-	-	-	-	-	M	-	F/F
		PM-09	PM	-	-	-	-	-	M	-	F/F
		PM-10	PM	-	-	-	-	-	M	-	F/F
		PM-11	PM	-	-	-	-	-	M	-	F/F
		PM-12	PM	-	-	-	-	-	M	-	F/F
		PM-13	PM	-	-	-	-	-	M	-	F/F
		PM-14	PM	-	-	-	-	-	M	-	F/F
		PM-15	PM	-	-	-	-	-	M	-	F/F
		PM-16	PM	-	-	-	-	-	M	-	F/F
SYS	4.3	SYS-01	Sys Interop	M	M	-	-	M	M	F/F	M
SYT	4.4	SYT-01	SI Tool	F	F	-	-	F	F	F/F	F
		SYT-02	SI Tool	F	F	-	-	F	F	F/F	F
		SYT-03	SI Tool	F	F	-	-	F	F	F/F	F
		SYT-04	SI Tool	F	F	-	-	F	F	F/F	F
		SYT-05	SI Tool	F	F	-	-	F	F	F/F	F
		SYT-06	SI Tool	F	F	-	-	F	F	F/F	F
		SYT-07	SI Tool	F	F	-	-	F	F	F/F	F
		SYT-08	SI Tool	F	F	-	-	F	F	F/F	F
		SYT-09	SI Tool	F	F	-	-	F	F	F/F	F
		SYT-10	SI Tool	F	F	-	-	F	F	F/F	F

Key:
M = Test or test area is mandatory for listed product type
F = Test or test area is feature dependent for list product type
- = Test or test area is not valid for listed product type

Table 1 - Test Requirements by Product Class

Test GRP	Sec #	Test Req.	Area	Device /Micro SATA HDD	Device ATAPI	Internal Cable Signal	Internal Cable Power	Host	Port Multi-plier *	eSATA Cable*	eSATA host/ device*
* -= Test or test area is currently documented as informative I = Denotes that this column has the same test as the corresponding internal column(s) to the left (host/device) -n = Suffix that denotes the test has changes from other columns (external changes to internal tests)											

3.1 General test requirements

3.1.1 Overview

All Serial ATA products under test shall meet the test requirements listed within this section (where applicable) to confirm Serial ATA interoperability relevant to the specified expected behavior.

3.1.2 GTR-01 – Software reset

3.1.2.1 Device expected behavior

See Section 11.4 of Serial ATA Revision 3.5.

Once the initial Register device-to-host FIS has been received and successfully acknowledged with no errors, a Device shall successfully respond to the setting of the SRST bit in the Device Control register at any time and perform the software reset protocol.

3.1.2.2 Measurement requirements

The required measurements are:

1) issue SRST to the device when no command is outstanding; and
2) repeat step 1 five times.

3.1.2.3 Pass/fail criteria

Verify Register FIS receipt (after reset sequence) from device with the appropriate signature contents in:

a) Sector Count;
b) LBA Low;
c) LBA Mid; and
d) LBA High registers.

NOTE 1 - See ATA/6 reference and correction e04127r0 within an allotted 31 s timeframe. These results shall be verified for all test instances.

3.1.3 GTR-02 – SATA Gen2 or above signaling speed backwards compatibility

3.1.3.1 Device expected behavior

See Section 17.5.7 of Serial ATA Revision 3.5.

If a device claims support for Serial ATA Gen2 or above (n ≥ 2) signaling speed (Word 76 bit 2 or above (n ≥ 2) set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data), then it shall also support Serial ATA signaling speed below it (< n) (Word 76 bit below n, (i.e., (n - 1) to 1 where: (n ≥ 2)) set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

In addition to verifying the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE contents, support shall be verified by ensuring compatibility and interoperability with Gen-1 and above up to Gen-n (n ≥ 2) host. Details on how this testing is done is not specified in this document.

3.1.3.2 Measurement requirements

The required measurements are:

1) if Word 76 bit 2 or above in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data is set to one when connected to a Gen-1 and above up to Gen-n (n ≥ 2) host, then continue to the next step, otherwise stop since this test is not applicable (na);
2) check Word 76 bit (n-1) to 1 where (n ≥ 2) in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data is set to one; and
3) complete OOB sequence at least ten times.

3.1.3.3 Pass/fail criteria

Values below shall be confirmed when tested in connection with Gen-1 and above up to Gen-n (n ≥ 2) host:

a) verify IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 76 bit 2 or above (n ≥ 2) set to one;
b) verify Word 76 bit below n, (i.e., (n-1) to 1) is set to one; and
c) verify Register FIS receipt (after each OOB sequence) from device with the appropriate signature contents in Sector Count, LBA Low, LBA Mid, and LBA High registers.

NOTE 2 - See ATA/6 reference and correction e04127r0.

3.1.4 GTR-03 – DMA protocol support

3.1.4.1 Device expected behavior

See Section 13.2 of Serial ATA Revision 3.5.

DMA support is able to be verified through Word 49 bit 8 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data. This bit shall be set to one for all Serial ATA devices.

The type of DMA supported is able to be verified through the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command data, Word 63, bits 2:0 for Multiword DMA (MWDMA) and Word 88 bits 5:0 for Ultra DMA (UDMA). If both types of DMA are supported, the UDMA type shall be selected. If only one type of DMA is supported, then the supported type shall be selected. The highest supported transfer rate of the selected DMA type shall be selected.

3.1.4.2 Measurement requirements

The required measurements are:

1) if Word 49 bit 8 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data is set to one, then run the appropriate tests below;

NOTE 3 - For consistency, the FCOMP pattern as defined in the Specification shall be used as the data set for the tests below. Some cases are dependent on transfer size so it may not be feasible to include complete iterations of the FCOMP pattern within the data set being used.

2) there are three different device types, each with their own test procedures:
   a) HDD:
      1) issue IDENTIFY DEVICE to device;
      2) issue and complete WRITE DMA command to device with transfer size of less than or equal to 8 Kbytes, followed by issue and completion of READ DMA command to device to the same disk location that the previous write was completed. The test shall verify that the contents read have the same values that were previously written;
      3) issue and complete WRITE DMA command to device with transfer size of greater than 8 Kbytes but less than or equal to 128 Kbytes, followed by issue and completion of READ DMA command to device to the same disk location that the previous write was completed. The test shall verify that the contents read have the same values that were written initially; and
      4) repeat the above 5 times;
   b) ATAPI device which only supports reading from media (e.g., CDROM, DVDROM, etc…):
      1) issue IDENTIFY PACKET DEVICE to device;

2) issue and complete one tracks worth of read commands using the DMA protocol with transfer size of less than or equal to 8 Kbytes, followed by issue and completion of another tracks worth of read commands using the DMA protocol to the same disk location that the previous reads were completed. The test shall verify that the contents read have the same values that were read initially;
3) issue and complete one tracks worth of read commands using the DMA protocol with transfer size of greater than 8 Kbytes but less than or equal to 128 Kbytes, followed by issue and completion of another tracks worth of read commands using the DMA protocol to the same disk location that the previous reads were completed. The test shall verify that the contents read have the same values that were read initially; and
4) repeat the above 5 times;

or

c) for ATAPI devices which support writing to media:
1) issue IDENTIFY PACKET DEVICE to device;
2) issue and complete one tracks worth of write commands using the DMA protocol with transfer size of less than or equal to 8 Kbytes, followed by issue and completion of one tracks worth of read commands using the DMA protocol to the same disk locations where the previous writes were completed. The test shall verify that the contents read have the same values that were previously written;
3) issue and complete one tracks worth of write commands using the DMA protocol with transfer size of greater than 8 Kbytes but less than or equal to 128 Kbytes, followed by issue and completion of one tracks worth of read commands using the DMA protocol to the same disk locations where the previous writes were completed. The test shall verify that the contents read have the same values that were previously written; and
4) repeat the above 5 times.

3.1.4.3 Pass/fail criteria

The pass/fail requirements are:
1) verify Word 49 bit 8 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE;
2) verify that data read is equal to data initially written (or read in case of ATAPI read-only device);
3) if neither MWDMA nor UDMA type is supported, then the result is fail; and
4) all five repetitions shall pass for this test to pass.

3.1.5 GTR-04 – General SATA support

3.1.5.1 Device expected behavior

See Section 13.2 of Serial ATA Revision 3.5.

For all Serial ATA devices, the entire contents of Word 93 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data shall be cleared to zero.

For all Serial ATA devices, the 1.5 Gbps interface rate shall be supported. This is able to be verified through Word 76 bit 1 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data. This bit shall be set to one for all Serial ATA devices.

If Word 76 is not 0000h or FFFFh, the device claims compliance with the Serial ATA Specification and supports the signaling rate indicated in bits 3:1. Since Serial ATA supports generational compatibility, multiple bits may be set. Bit 0 is reserved and shall be cleared to zero (thus a Serial ATA device has at least one bit cleared in this field and at least one bit set providing clear differentiation).

Word 77..79 bit 0 shall be cleared to zero.

3.1.5.2 Measurement requirements

Issue IDENTIFY DEVICE or IDENTIFY PACKET DEVICE to device.

3.1.5.3 Pass/fail criteria

The pass/fail requirements are:

1) verify Word 93 is cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE;
2) verify Word 76 bit 1 is set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE; and
3) verify Word 76..79 bit 0 is cleared to zero.

3.1.6 GTR-05 : Unrecognized FIS receipt (informative)

3.1.6.1 Device expected behavior

See Section 10.5.2.2 of Serial ATA Revision 3.5.

Upon receipt of an “unrecognized FIS”, the receiver shall follow the link layer state machine definitions in Section 10.7 of the Serial ATA Revision 3.5. The expected response is status return with an R_ERR.

> NOTE 4 - Determination of any FIS being “unrecognized” is done by the recipient of the FIS. The contents of the “Unrecognized FIS” are not defined by this document, but shall be described in each applicable MOI.

3.1.6.2 Measurement requirements

Transmit undefined FIS to device.

3.1.6.3 Pass/fail criteria

Verify R_ERR response from device.

3.2 Native command queuing

3.2.1 Overview

The Native Command Queuing (NCQ) test requirements are determined by the requirements of the feature as defined in Serial ATA Revision 3.5.

All of the tests listed in this section require that support for NCQ is claimed by the product for verification of the expected behavior. Support for NCQ is verified by reading Word 76 bit 8 set to one in IDENTIFY DEVICE data.

3.2.2 NCQ-01 : Forced unit access

3.2.2.1 Device expected behavior

See Section 11.15 and Section 13.6.5 of Serial ATA Revision 3.5.

Devices that support the NCQ commands (READ FPDMA QUEUED and WRITE FPDMA QUEUED) shall support the Force Unit Access (FUA) bit.

For WRITE FPDMA QUEUED when the FUA bit is set to one, the data shall be written to the storage media before completing the command. Due to the limitations in testability of specific device functions, this test shall be limited to verifying the compatibility of a device in receiving a command with the FUA bit set to one. This test shall not completely verify whether data was written to non-volatile media.

3.2.2.2 Measurement requirements

The requirements are:
1) if Word 76 bit 8 in IDENTIFY DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;
2) issue and complete WRITE FPDMA QUEUED with FUA bit set to one; and
3) issue and complete READ FPDMA QUEUED to the same disk location.

3.2.2.3 Pass/fail criteria

Verify that data read is equal to data written.

3.2.3 NCQ-02 : Read log ext log page 10h support

3.2.3.1 Device expected behavior

See Section 13.7.10.2.11 of Serial ATA Revision 3.5.

If a device claims support for Native Command Queuing (Word 76 bit 8 set to one in IDENTIFY DEVICE data), then it shall also support READ LOG EXT log page 10h and the General Purpose Logging feature set. Support for READ LOG EXT log page 10h is reflected in the General Purpose Log Directory page (log page 0) by having the value 1 at offset 20h and the value 0 at offset 21h of that log page to indicate existence of a log page at address 10h of 1-page in length.

A READ LOG EXT log page 10h command shall be issued and completed without error. No contents shall be validated.

3.2.3.2 Measurement requirements

The required measurements are:

1) if Word 76 bit 8 in IDENTIFY DEVICE is set to one and Word 87 bit 5 in IDENTIFY DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;
2) issue READ LOG EXT to log page 00h; and
3) issue READ LOG EXT to log page 10h.

3.2.3.3 Pass/fail criteria

The pass/fail requirements are:

1) verify successful completion & data transfer for log page 0h;
2) verify offset 20h of log page 00h contains value of 1;
3) verify offset 21h of log page 00h contains value of 0; and
4) verify successful completion and data transfer for log page 10h, it is *not* necessary that the contents of the log page are verified for specific values.

3.2.4 NCQ-03 : Intermix of legacy and NCQ commands

3.2.4.1 Device expected behavior

See Section 13.6.3 of Serial ATA Revision 3.5.

Upon receiving a legacy ATA command while a native queued command is outstanding, an error has occurred, and the device shall perform necessary state cleanup to return to a state with no commands pending. Legacy ATA commands include all commands other than the READ FPDMA QUEUED and WRITE FPDMA QUEUED commands.

The device shall signal the error condition to the host by transmitting a Register FIS to the host with the ERR bit set to one and the BSY bit cleared to zero in the Status field, and the ABRT bit set to one in the Error field. Upon detecting an error when there are one or more NCQ commands outstanding, the device shall stop processing commands until a READ LOG EXT command with a specified log page of 10h or reset is issued. Upon receipt of the READ LOG EXT command, the device shall send a Set Device Bits FIS to discard all commands in the pending device queue, followed by data for the log page. The READ LOG EXT page shall reflect that the error condition was a result of a legacy ATA command having been issued by having the NQ bit set to one. The device shall not continue command processing for any of the outstanding commands following this error.

If no prior NCQ error has occurred and a device has received a READ LOG EXT command while there are NCQ commands outstanding, the device shall respond as described above as having received a legacy ATA command while one or more native queued commands are outstanding.

3.2.4.2 Measurement requirements

The required measurements are:

1) if Word 76 bit 8 in IDENTIFY DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;

2) check Word 75 bits 4:0 to verify maximum queue depth reported by device;
3) issue at least X random FPDMA QUEUED commands (read or write), where X is the maximum queue depth reported above;
4) issue a legacy ATA command using each of the following:
    1) IDENTIFY DEVICE;
    2) PIO write;
    3) DMA read; and
    4) Read Log Ext with log page 10h;

NOTE 5 - The test shall be run a total of four times to ensure each legacy ATA command listed above is used for the test.

5) verify Register FIS receipt with:
    1) ERR bit set to one;
    2) DRDY bit set to one;
    3) DF bit cleared to zero;
    4) BSY bit cleared to zero; and
    5) DRQ bit cleared to zero;
    and
6) issue Read Log Ext to log page 10h.

3.2.4.3 Pass/fail criteria

The pass/fail requirements are:
1) verify receipt of Register FIS with error;
2) verify:
    1) SDB receipt with ERR bit cleared to zero;
    2) DRDY set to one;
    3) DF bit cleared to zero;
    4) BSY bit cleared to zero;
    5) DRQ bit cleared to zero;
    6) 'I' bit cleared to zero; and
    7) SActive field set to FFFF FFFFh;
3) verify that the NQ bit is set to one in the data within log page 10h; and
4) verify that the checksum is correct in the data within Log page 10h.

NOTE 6 – There is opportunity for a device to complete all outstanding commands prior to the host being able to send the legacy ATA command. In these cases, the device shall not be failed for this particular test.

3.2.5 NCQ-04 : Device response to malformed NCQ command

3.2.5.1 Device expected behavior

See Section 13.6.3 and Section 13.6.5.1 of Serial ATA Revision 3.5.

Malformed commands have the possibility of including the following situations:
a) specified LBA is out of the device supported range;
b) duplicate tag value for outstanding NCQ command; or
c) TAG value is out of the device supported range, only in the case that the device reports support for less than 32 outstanding commands.

In response to a malformed READ FPDMA QUEUED or WRITE FPDMA QUEUED command due to a duplicate tag or out of range tag, the device shall transmit a Register FIS to the host with the ERR bit set to one, and the BSY bit cleared to zero in the Status register. The 'I' bit shall be set to one. The ABRT bit shall be set to one in the Error field. The device shall stop processing commands until a READ LOG EXT command with a specified log page of 10h or reset is issued. Upon receipt of the READ LOG EXT command, the device shall send a Set Device Bits FIS to discard all commands in the pending device queue, followed by data for the log page. The READ LOG EXT page shall have the NQ bit cleared to

zero. The TAG field within the log page shall contain the tag associated with the NCQ command which failed.

In response to a malformed READ FPDMA QUEUED or WRITE FPDMA QUEUED command due to an LBA out of range, the device may report the error in one of two ways:

a) transmit a Register FIS to the host with the ERR bit set to one, and the BSY bit cleared to zero in the Status register. The 'I' bit shall be set to one. Either the ABRT bit or IDNF bit shall be set to one in the Error field. The device shall stop processing commands until a READ LOG EXT command with a specified log page of 10h or reset is issued. Upon receipt of the READ LOG EXT command, the device shall send a Set Device Bits FIS to discard all commands in the pending device queue, followed by data for the log page. The READ LOG EXT page shall have the NQ bit cleared to zero. The TAG field within the log page shall contain the tag associated with the NCQ command which failed; or

b) if the device accepts the command, then the device shall report the error within a subsequent Set Device Bits FIS. A Set Device Bits FIS shall be transferred with the ERR bit set to one, and the BSY bit cleared to zero in the Status register. The 'I' bit shall be set to one. Either the ABRT bit or IDNF bit shall be set to one in the Error field. The device shall stop processing commands until a READ LOG EXT command with a specified log page of 10h or reset is issued. Upon receipt of the READ LOG EXT command, the device shall send a Set Device Bits FIS to discard all commands in the pending device queue, followed by data for the log page. The READ LOG EXT page shall have the NQ bit cleared to zero. The TAG field within the log page shall contain the tag associated with the NCQ command which failed.

3.2.5.2 Measurement requirements

The required measurements are:

1) if Word 76 bit 8 in IDENTIFY DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;
2) issue an FPDMA command with each of the following:
    1) LBA out of range (refer to Words 60..61/Words 100..103 in IDENTIFY DEVICE data);
    2) duplicate tag for another outstanding NCQ command (shall require other outstanding NCQ commands); and
    3) tag value out of device supported range (refer to Word 75 bits 4:0 in IDENTIFY DEVICE data);

    NOTE 7 – The above test shall be run a total of three times to ensure each type of command listed above is used for the test.

3) After each of the above:
    a) if a Register FIS receipt with Error, then issue Read Log Ext to log page 10h; or
    b) if a Register FIS is not received with Error, an SDB FIS receipt posting the error shall be expected so issue Read Log Ext to log page 10h.

3.2.5.3 Pass/fail criteria

The pass/fail requirements are:

1) in the case of a duplicate tag or tag out of range, verify the following:
    1) receipt of Register FIS with error;
    2) SDB receipt with:
        1) ERR bit cleared to zero;
        2) DRDY bit set to one;
        3) DF bit cleared to zero;
        4) 'I' bit cleared to zero; and
        5) SActive field set to FFFF FFFFh;
    3) verify within Log page 10h:
        1) TAG field includes the tag associated with the failed NCQ command;
        2) NQ bit cleared to zero;
        3) ERR bit set to one;

4) DRDY is set to one;
5) DF bit cleared to zero; and
6) ABORT set to one;
and
4) verify that the checksum is correct in the data within Log page 10h;
2) in the case of LBA out of range, verify:
1) receipt of Register FIS with error;
2) SDB receipt with:
1) ERR bit cleared to zero;
2) DRDY bit set to one;
3) DF bit cleared to zero;
4) 'I' bit cleared to zero; and
5) SActive field set to FFFF FFFFh;
3) TAG field includes the tag associated with the failed NCQ command in the data within log page 10h;
4) LBA address in the data within Log page 10h is the LBA address issued in NCQ command;
5) within Log page 10h verify:
1) NQ bit is cleared to zero;
2) ERR bit is set to one;
3) DRDY is set to one;
4) DF bit is cleared to zero; and
5) ABORT or IDNF is set to one in the data;
and
6) verify that the checksum in the data page is correct;
3) in the case of the receipt of SDB FIS with error verify:
1) ERR bit cleared to zero;
2) DRDY bit set to one;
3) DF bit cleared to zero;
4) 'I' bit cleared to zero;
5) SActive field set to FFFF FFFFh;
6) in Log page 10h verify:
1) TAG field includes the tag associated with the failed NCQ command;
2) LBA address is the LBA address issued in NCQ command;
3) NQ bit is cleared to zero;
4) ERR bit is set to one;
5) DRDY is set to one;
6) DF bit is cleared to zero;
7) ABORT or IDNF is set to one; and
8) checksum is correct for the data.

3.2.6 NCQ-05 : DMA setup auto-activate

3.2.6.1 Device expected behavior

See Section 10.5.9 of Serial ATA Revision 3.5.

To test for this test requirement, the device shall claim support for DMA Setup Auto-Activate (IDENTIFY DEVICE data, Word 78 bit 2 set to one) and have the feature enabled using the SET FEATURES command (IDENTIFY DEVICE data, Word 79 bit 2 set to one).

A device shall not transmit a DMA Activate FIS to trigger transmission of the first Data FIS from the host, if it had previously sent a DMA Setup FIS with the Auto-Activate bit 'A' set to one.

3.2.6.2 Measurement requirements

The required measurements are:

1) if Word 76 bit 8 in IDENTIFY DEVICE is set to one and Word 78 bit 2 in IDENTIFY DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;
2) issue SET FEATURES with:
   a) Features value of 10h; and
   b) Sector Count value of 02h;
3) check Word 79 bit 2 in IDENTIFY DEVICE; and
4) issue WRITE FPDMA QUEUED with Auto-Activate bit set to one.

3.2.6.3 Pass/fail criteria

The pass/fail requirements are:
1) verify Word 78 bit 2 of IDENTIFY DEVICE is set to one;
2) verify Word 79 bit 2 of IDENTIFY DEVICE is set to one (following SET FEATURES);
3) verify Initial DMA Activate FIS is indeed missing prior to first transmitted Data FIS; and
4) verify command completion (data transferred and Register FIS received).

3.3 Asynchronous signal recovery

3.3.1 ASR-01 : COMINIT response interval

3.3.1.1 Device expected behavior

See Section 15.2.2.2 of Serial ATA Revision 3.5.

In a case where the device is in an interface quiescent state in response to receipt of a COMRESET signal from the host, the device shall respond with a COMINIT signal within 10 ms of de-qualification of a received COMRESET signal.

3.3.1.2 Measurement requirements

The required measurements are:
1) setup bus analyzer (or scope) for tracing of bus activity & begin tracing;
2) power on host & device;
3) initiate COMRESET sequence; and
4) repeat step 3 five times.

3.3.1.3 Pass/fail criteria

Confirm OOB sequence completion and COMINIT timing beings within 10 ms of COMRESET receipt from host (use trace to analyze timings). Since a single result is reported, the worst-case result out of all 5 cases shall be reported (i.e., largest value).

> NOTE 8 - The time to be compared is from the end of the COMRESET burst (detectable point) to the start of COMINIT burst from the device. Some subtraction or modification to a result displayed by a bus analyzer may be necessary to extract the appropriate value for comparison.

3.3.2 ASR-02 : COMINIT OOB interval

3.3.2.1 Device expected behavior

See Section 8.2 of Serial ATA Revision 3.5.

When Phy communication is not established, the device shall not initiate a new OOB (COMINIT) to the host faster than every 10 ms.

3.3.2.2 Measurement requirements

The required measurements are:
1) setup bus analyzer (or scope) for tracing of bus activity & begin tracing;
2) power on host & device;
3) power off host, keeping device powered on; and
4) repeat step 3 ten times.

3.3.2.3 Pass/fail criteria

Verify that once host is powered off, that device sends COMINIT repeatedly and no faster than every 10 ms (use trace to verify behavior and timings). Since a single result is reported, the worst-case result out of all 10 cases shall be reported (i.e., smallest value).

> NOTE 9 - The time to be compared is from the start of the first COMINIT burst (detectable point) to the start of a subsequent COMINIT burst from the device. Some subtraction or modification to a result displayed by a bus analyzer may be necessary to extract the appropriate value for comparison.

3.3.3 ASR-03 : COMRESET OOB interval

3.3.3.1 Host expected behavior

See Section 8.4.2 of Serial ATA Revision 3.5.

When Phy communication is not established, the host shall not initiate a new OOB (COMRESET) to the device faster than every 10 ms.

3.3.3.2 Measurement requirements

The required measurements are:

1) setup bus analyzer (or scope) for tracing of bus activity & begin tracing;
2) power on host & device;
3) power off device, keeping host powered on; and
4) repeat step 3 ten times.

3.3.3.3 Pass/fail criteria

Verify that once device is powered off, that host sends COMRESET repeatedly and no faster than every 10 ms (use trace to verify behavior and timings). Since a single result is reported, the worst-case result out of all 10 cases shall be reported (i.e., smallest value).

> NOTE 10 - The time to be compared is from the start of the first COMRESET burst (detectable point) to the start of a subsequent COMRESET burst from the host. Some subtraction or modification to a result displayed by a bus analyzer may be necessary to extract the appropriate value for comparison.

3.4 Software settings preservation

3.4.1 Testing requirements

All of the test requirements listed in this section require that support for Software Settings Preservation is claimed by the product for verification of the Expected behavior. Support for Software Settings Preservation is able to be verified by reading Word 78 bit 6 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data.

See Section 13.5 of Serial ATA Revision 3.5 for details on Software Settings Preservation.

3.4.2 SSP-01 : Initialize device parameters

3.4.2.1 Device expected behavior

This test is not applicable to ATAPI devices.

This test is only valid for a device that where the values contained in Words 54..58 are valid (Word 53 bit 0 set to one in IDENTIFY DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the device settings established by the INITIALIZE DEVICE PARAMETERS command. Specifically, the values contained within Words 58..54 in IDENTIFY DEVICE data shall be maintained after a COMRESET. The value contained within Word 53 bit 0 in IDENTIFY DEVICE data shall also be maintained after a COMRESET.

3.4.2.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 6 in IDENTIFY DEVICE is set to one and also Word 53 bit 0 is set to one, then continue to step 2, otherwise stop since this test is not required;
2) save values of device settings (Words 58..54);
3) issue COMRESET and complete OOB sequence; and
4) compare values of device settings (Words 58..54).

3.4.2.3 Pass/fail criteria

Verify that IDENTIFY DEVICE Words 58..54 contain the same values before and after COMRESET.

3.4.3 SSP-02 : Read/write stream error log

3.4.3.1 Device expected behavior

This test is not applicable to ATAPI devices.

This test is only valid if a device claims support for Streaming (Word 84 bit 4 set to one in IDENTIFY DEVICE data).

Upon the receipt of a COMRESET, a device shall maintain the Read Stream Error Log and Write Stream Error Log contents. Specifically, the values contained within log pages 21..22 shall be maintained after a COMRESET.

3.4.3.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 6 in IDENTIFY DEVICE is set to one and also Word 84 bit 4 is set to one, then continue to the next step, otherwise stop since this test is na;
2) save values of log pages 21..22;
3) complete an ATA Specification compliant activity to change the values represented in log pages 21..22 such that they do not represent the default values;
4) verify the new values of log pages 21..22 do not match the saved values;
5) issue COMRESET and complete OOB sequence; and
6) compare new values of log pages 21..22 to newest saved values.

3.4.3.3 Pass/fail criteria

Verify that log pages 21..22 contain the same values before and after COMRESET.

3.4.4 SSP-03 : Security mode state

3.4.4.1 Device expected behavior

This test is only valid if a device claims support for Security Mode (Word 82 bit 1 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of Security Mode. Specifically, if Security Mode is enabled (Word 85 bit 1 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET, then the mode value (Word 128 bits 3:1 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) shall be maintained after a COMRESET.

3.4.4.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one, Word 82 bit 1 is set to one, and Word 85 bit 1 is cleared to zero, then continue to the next step, otherwise stop since this test is na;
2) save values of Word 128 bits 3:1;
3) complete an ATA Specification compliant activity to change the values represented in Word 128 bits 3:1;
4) verify the values of Word 128 bits 3:1 have changed;

5) issue the following commands to make sure the device works in SEC5 state:
   a) for ATA device, issue Read DMA and Write Sector, these commands shall complete successfully; or
   b) for ATAPI device, issue Inquiry, it shall complete successfully;
6) issue COMRESET and complete OOB sequence;
7) verify value of Word 85 bit 1 is set to one;
8) compare value of Word 128 bits 3:1 to saved values; and
9) issue the following commands to make sure the device works in SEC5 state instead of SEC4 state:
   a) for ATA device, issue Read DMA and Write Sector, these commands shall complete successfully; or
   b) for ATAPI device, issue Inquiry, it shall complete successfully.

3.4.4.3 Pass/fail criteria

The pass/fail requirements are:

1) verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 85 bit 1 contains the same value following COMRESET;
2) verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 128 bits 3:1 contain the same value following COMRESET; and
3) if the commands issued before COMRESET do not complete successfully, then the test result for command process is na, otherwise verify the commands issued after COMRESET completed successfully.

3.4.5 SSP-04 : Set address max

3.4.5.1 Device expected behavior

This test is not applicable to ATAPI devices.

This test is only valid for a device that claims support for Host Protected Area (Word 82 bit 10 set to one in IDENTIFY DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the max address established by the SET MAX ADDRESS or SET MAX ADDRESS EXT command. Specifically, the value contained within Words 60..61 in IDENTIFY DEVICE data shall be maintained after a COMRESET.

If 48-bit support is enabled by the device (Word 83 bit 10 set to one in IDENTIFY DEVICE data), then the values contained within Words 100..103 in IDENTIFY DEVICE data shall also be maintained after a COMRESET.

3.4.5.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 6 in IDENTIFY DEVICE is set to one and also Word 82 bit 10 in IDENTIFY DEVICE is set to one, then proceed continue to the next step, otherwise stop since this test is na;
2) issue READ NATIVE MAX ADDRESS (or READ NATIVE MAX ADDRESS EXT) to get max user accessible address;
3) issue SET MAX ADDRESS (or SET MAX ADDRESS EXT) with new valid max accessible address;
4) save values of Words 60..61;
5) if Word 83 bit 10 is set to one, also save values of Words 100..103;
6) verify correct address is set due to SET MAX ADDRESS (EXT) command;
7) issue COMRESET and complete OOB sequence;
8) compare IDENTIFY DEVICE Words 60..61 to saved values; and
9) if Word 83 bit 10 is set to one, compare Words 100..103 to saved values.

3.4.5.3 Pass/fail criteria

The pass/fail requirements are:

1) verify that IDENTIFY DEVICE Words 60..61 contain the same values before and after COMRESET; and
2) if Word 83 bit 10 is set to one, verify that Words 100..103 contain the same values before and after COMRESET.

3.4.6 SSP-05 : Set features – Write cache enable/disable

3.4.6.1 Device expected behavior

This test is only valid for a device that claims support for Write Cache (Word 82 bit 5 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of write cache enable/disable. Specifically, if write cache is enabled (Word 85 bit 5 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET, then the feature shall be enabled after the COMRESET. If write cache is disabled (Word 85 bit 5 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET, then the feature shall be disabled after the COMRESET.

3.4.6.2 Measurement requirements

The required measurements are:
1) if Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one and Word 82 bit 5 is set to one, then continue to the next step, otherwise stop since this test is na;
2) save value of Word 85 bit 5;
3) issue SET FEATURES to alter setting for Write Cache enable/disable;
4) issue COMRESET and complete OOB sequence; and
5) compare value of Word 85 bit 5 to saved value.

3.4.6.3 Pass/fail criteria

Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 85 bit 5 contains the same value following COMRESET.

3.4.7 SSP-06 : Set features – set transfer mode

3.4.7.1 Device expected behavior

Upon receipt of a COMRESET, a device shall maintain the Multiword DMA and Ultra DMA mode settings. Specifically, the values contained within Word 63 bits 10:8 (MWDMA) and Word 88 bits 14:8 (UDMA) in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data shall be maintained after a COMRESET.

The bits in Word 88 are only valid if Word 53 bit 2 is set to one.

3.4.7.2 Measurement requirements

The required measurements are:
1) if Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;
2) save values of Word 63 bits 10:8 for Multiword DMA support;
3) save values of Word 88 bits 14:8 for Ultra DMA support;
4) complete an ATA Specification compliant activity to change the values represented in Word 63 bits 10:8 and Word 88 bits 14:8 such that they do not represent the default values;
5) verify the new values of Word 63 bits 10:8 and Word 88 bits 14:8;
6) issue COMRESET and complete OOB sequence;

   NOTE 11 - You may need to appropriately handle the reset condition for ATAPI devices (i.e., handling of request sense).

7) compare values of Word 63 bits 10:8;
8) compare values of Word 88 bits 14:8;

9) issue a read to any valid random location on the device (using Multiword DMA transfer, if supported); and
10) issue a read to any valid random location on the device (using Ultra DMA transfer, if supported).

3.4.7.3 Pass/fail criteria

The pass/fail requirements are:
1) verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 63 bits 10:8 contain the same values before and after COMRESET;
2) verify that Word 88 bits 14:8 contain the same values before and after COMRESET;
3) if supported, verify that the read Multiword DMA command completed successfully; and
4) if supported, verify that the read Ultra DMA command completed successfully.

3.4.8 SSP-07 : Set features – Advanced power management enable/disable

3.4.8.1 Device expected behavior

This test is not applicable to ATAPI devices.

This test is only valid for a device that claim support for Advanced Power Management (Word 83 bit 3 set to one in IDENTIFY DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of Advanced Power Management (APM) enable/disable and the advanced power management level. Specifically, if APM is enabled (Word 86 bit 3 set to one in IDENTIFY DEVICE data) upon receipt of a COMRESET, then the feature shall be enabled after the COMRESET, and Word 91 bits 7:0 in IDENTIFY DEVICE data shall contain the value present prior to the COMRESET. If APM is disabled (Word 86 bit 3 cleared to zero in IDENTIFY DEVICE data) upon receipt of a COMRESET, then the feature shall be disabled after the COMRESET.

3.4.8.2 Measurement requirements

The required measurements are:
1) if Word 78 bit 6 in IDENTIFY DEVICE is set to one and Word 83 bit 3 is set to one, then continue to the next step, otherwise stop since this test is na;
2) verify Word 86 bit 3 is set to one;
3) issue SET FEATURES to alter setting for APM enable/disable;
4) if Word 86 bit 3 is set to one, then save value of Word 91 bits 7:0;
5) issue COMRESET and complete OOB sequence;
6) verify Word 83 bit 3 is set to one; and
7) if Word 86 bit 3 is set to one, then compare values of Word 91 bits 7:0 to saved values.

3.4.8.3 Pass/fail criteria

The pass/fail requirements are:
1) verify that IDENTIFY DEVICE Word 86 bit 3 contains the same value following COMRESET; and
2) if Word 86 bit 3 was set to one, verify that IDENTIFY DEVICE 91 bits 7:0 contains the same values following COMRESET.

3.4.9 SSP-08 : Set features – read look-ahead

3.4.9.1 Device expected behavior

This test is only valid for a device that claims support for look-ahead (Word 82 bit 6 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of look-ahead enable/disable. Specifically, if support for look-ahead is enabled (Word 85 bit 6 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET, then the feature shall be enabled after the COMRESET. If support for look-ahead is disabled (Word 85 bit 6 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET, then the feature shall be disabled after the COMRESET.

3.4.9.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one and Word 82 bit 6 is set to one, then continue to the next step, otherwise stop since this test is na;
2) save the value of Word 85 bit 6;
3) issue SET FEATURES to alter setting for read look-ahead enable/disable;
4) issue COMRESET and complete OOB sequence; and
5) compare the value of Word 85 bit 6 to the saved value.

3.4.9.3 Pass/fail criteria

Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 85 bit 6 contains the same value before and after COMRESET.

3.4.10 SSP-09 : Set features – release interrupt

3.4.10.1 Device expected behavior

This test is only valid for a device that claims support for release interrupt (Word 82 bit 7 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of release interrupt enable/disable. Specifically, if support for release interrupt is enabled (Word 85 bit 7 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET, then the feature shall be enabled after the COMRESET. If support for release interrupt is disabled (Word 85 bit 7 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET, then the feature shall be disabled after the COMRESET.

3.4.10.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one and Word 82 bit 7 is set to one, then continue to the next step, otherwise stop since this test is na;
2) save value of Word 85 bit 7;
3) issue SET FEATURES to alter setting for release interrupt enable/disable;
4) issue COMRESET and complete OOB sequence; and
5) compare value of Word 85 bit 7 to saved value.

3.4.10.3 Pass/fail criteria

Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 85 bit 7 contains the same value before and after COMRESET.

3.4.11 SSP-10 : Set features – service interrupt

3.4.11.1 Device expected behavior

This test is only valid for a device that claims support for service interrupt (Word 82 bit 8 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of service interrupt enable/disable. Specifically, if support for service interrupt is enabled (Word 85 bit 8 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET, then the feature shall be enabled after the COMRESET. If support for service interrupt is disabled (Word 85 bit 8 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET, then the feature shall be disabled after the COMRESET.

3.4.11.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE set to one and Word 82 bit 8 is set to one, then continue to the next step, otherwise stop since this test is na;
2) save value of Word 85 bit 8;

3) issue SET FEATURES to alter setting for service interrupt enable/disable;
4) issue COMRESET and complete OOB sequence; and
5) compare value of Word 85 bit 8 to saved value.

3.4.11.3 Pass/fail criteria

Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 85 bit 8 contains the same value before and after COMRESET.

3.4.12 SSP-11 : Set multiple mode (informative)

3.4.12.1 Device expected behavior

This test is not applicable to ATAPI devices.

This test is only valid for a device that claims the maximum number of logical sectors per DRQ data block (Word 47 bits 7:0 are non-zero).

Upon receipt of a COMRESET, a device shall maintain the block size established by the Set Multiple Mode command. Specifically, the value contained within Word 59 bits 8:0 in IDENTIFY DEVICE data shall be maintained after a COMRESET.

3.4.12.2 Measurement requirements

The required measurements are:
1) if Word 78 bit 6 in IDENTIFY DEVICE is set to one and Word 47 bits 7:0 are a non-zero value, then continue to the next step, otherwise stop since this test is na;
2) issue Set Multiple command to change the multiple sector setting from the default setting;
3) save the value of Word 59 bits 8:0;
4) verify correct multiple sector setting is set due to Set Multiple command;
5) issue COMRESET and complete OOB sequence; and
6) compare value of Word 59 bits 8:0 to the saved value.

3.4.12.3 Pass/fail criteria

Verify that IDENTIFY DEVICE Word 59 bits 8:0 contain the same value before and after COMRESET.

3.4.13 SSP-12 : Set features – write-read-verify

3.4.13.1 Device expected behavior

This test is not applicable to ATAPI devices.

This test is only valid for a device that claims support for Write-Read-Verify (Word 119 bit 1 set to one in IDENTIFY DEVICE data).

For the contents of IDENTIFY DEVICE data Word 120 bit 1, Words 210..211, and Word 220 bits 7:0, the device shall not return to its Write-Read-Verify factory default setting after processing a COMRESET.

3.4.13.2 Measurement requirements

The required measurements are:
1) if Word 86 bit 15 in IDENTIFY DEVICE is set to one and Word 119 bit 1 in IDENTIFY DEVICE is set to one, Word 78 bit 6 in IDENTIFY DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;
2) save default values of:
   a) disable/enable state of Write-Read-Verify;
   b) Write-Read-Verify mode; and
   c) Write-Read-Verify sector;
3) issue SET FEATURE to change the disable/enable state of Write-Read-Verify, Write-Read-Verify mode, and Write-Read-Verify sector count for Mode 3 from their default factory settings;
4) if no new setting is able to be supported by the device except its default factory setting, this test is not applicable;

5) issue COMRESET and complete OOB sequence; and
6) compare the values of Word 120 bit 1, Words 210..211, and Word 220 bits 7:0 to the saved values.

NOTE 12 - If the device supports multiple modes and/or multiple sector count for Mode 3 except its default factory setting, then repeat the above test for all the available settings.

3.4.13.3 Pass/fail criteria

Verify that the contents in Word 120 bit 1, Words 210..211, and Word 220 bits 7:0, which have been changed from their default factory settings, contain the same values before and after COMRESET.

3.4.14 SSP-13 : Set features – DIPM enable/disable

3.4.14.1 Device expected behavior

This test is only valid for a device that claims support for DIPM (Word 78 bit 3 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) and DIPM SSP (Word 78 bit 10 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of DIPM enable/disable. Specifically, if DIPM is enabled (Word 79 bit 3 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET, then the feature shall be enabled after the COMRESET. If DIPM is disabled (Word 79 bit 3 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET, then the feature shall be disabled after the COMRESET.

3.4.14.2 Measurement requirements

The required measurements are:
1) if Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one and both Word 78 bit 3 and bit 10 are set to one, then continue to the next step, otherwise stop since this test is na;
2) save value of Word 79 bit 3;
3) issue SET FEATURES to alter setting for DIPM enable/disable;
4) issue COMRESET and complete OOB sequence;
5) compare value of Word 79 bit 3 to saved value; and
6) repeat the above sequences to verify both the enabled and disabled state.

3.4.14.3 Pass/fail criteria

Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 79 bit 3 contains the same value following COMRESET.

3.4.15 SSP-14 : Set features – DeviceSleep enable/disable

3.4.15.1 Device expected behavior

This test is only valid for a device that claims support for DeviceSleep (Word 78 bit 8 set to one in IDENTIFY DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of DeviceSleep enable/disable. Specifically, if DeviceSleep is enabled (Word 79 bit 8 set to one in IDENTIFY data) upon receipt of a COMRESET, then the feature shall be enabled after the COMRESET. If DeviceSleep is disabled (Word 79 bit 8 cleared to zero in IDENTIFY DEVICE data) upon receipt of a COMRESET, then the feature shall be disabled after the COMRESET.

Also the value of Qword 2 Bit 10 in Serial ATA Log is consistent to the one of Word 79 bit 8 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data.

3.4.15.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 6 in IDENTIFY DEVICE is set to one and Word 78 bit 8 is set to one, then continue to the next step, otherwise stop since this test is na;
2) save value of Word 79 bit 8 in IDENTIFY DEVICE;
3) save value of Qword 2 Bit 10 in Serial ATA Log;
4) issue SET FEATURES to alter setting for DeviceSleep enable/disable;
5) issue COMRESET and complete OOB sequence;
6) compare value of Word 79 bit 8 in IDENTIFY DEVICE to the saved value;
7) compare value of Qword 2 Bit 10 in Serial ATA Log to the saved value; and
8) repeat the above sequences to verify both the enabled and disabled state.

3.4.15.3 Pass/fail criteria

Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 79 bit 8 and Serial ATA Log Qword 2 Bit 10 contains the same value following COMRESET.

3.5 Interface power management

3.5.1 Overview

Some of the tests listed in this section require that support for device initiating interface power management and/or host initiating interface power management is claimed by the product for verification of the expected behavior. Support for device initiating interface power management is able to be verified by reading Word 78 bit 3 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data. Support for host initiating interface power management is able to be verified by reading Word 76 bit 9 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data. For each test requirement, there shall be a note outlining whether support for device initiating interface power management and/or host initiating interface power management is a requirement for testing said test requirement.

A product may claim support for both device initiating interface power management (DIPM) requests and receipt of host initiating power management (HIPM) requests. It is not required to support both types of requests.

If a host intends to be validated for Interface Power Management (IPM) support through the Interoperability Tests, it is required to be pre-configured (BIOS, driver, utility) to automatically send SET FEATURES to enable DIPM requests following device detection and to configure the host in such a way that it may accept DIPM requests. This is because there are limitations to ways hosts may be validated for a feature, and DIPM requests are a key requirement for any IPM validation for a host. If a host only supports HIPM, there is no way to validate this support and it shall not be verified for Interop Testing.

3.5.2 IPM-01 : Partial state exit latency (host-initiated)

3.5.2.1 Device/host expected behavior

See Section 8.1 of Serial ATA Revision 3.5.

The device and host exit latency (i.e., COMWAKE response) from the partial state shall start within 10 us of COMWAKE receipt from the initiator of the wake sequence.

3.5.2.2 Measurement requirements (Device)

The required measurements are:
1) if Word 76 bit 9 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;
2) setup a bus analyzer (or scope) for tracing of bus activity and begin tracing;
3) issue PMREQ_P and receive device response;
4) issue COMWAKE and wait for complete wake of device;
5) issue IDENTIFY DEVICE or IDENTIFY PACKET DEVICE; and
6) repeat the above 10 times.

3.5.2.3 Pass/fail criteria (Device)

The pass/fail requirements are:

1) confirm Partial wake sequence completion and COMWAKE timing of being within 10 us of COMWAKE receipt from host (use trace to analyze timings);
2) the device shall process the DEVICE or IDENTIFY PACKET DEVICE correctly after the complete wake of the device; and
3) the worst-case time out of 10 repetitions shall be reported (i.e., largest value).

3.5.2.4 Measurement requirements (Host)

The required measurements are:

1) setup bus analyzer (or scope) for tracing of bus activity and begin tracing;
2) wait for a Partial IPM request from the host;

   NOTE 13 – There is no guaranteed method for causing the host to send a request. A common ATA (or vendor specific) method which may cause a request from the host is to leave the system idle (up to 10 s).
   NOTE 14– Ensure there is no conflict with a device initiated request.
   NOTE 15– A host vendor may provide a vendor unique tool for initiating the power management requests as to ensure the test does complete as necessary.

3) issue COMWAKE and wait for complete wake of host; and
4) repeat the above 10 times.

3.5.2.5 Pass/fail criteria (Host)

The pass/fail requirements are:

1) confirm partial wake sequence completion and host transmission of ALIGNp within 10 us of COMWAKE receipt from device/emulator/tool (use trace to analyze timings); and

   NOTE 16 - In the case that no host initiated request was completed, the pass/fail result shall be na.

2) the worst-case time out of 10 repetitions shall be reported (i.e., largest value).

3.5.3 IPM-02 : Slumber state exit latency (host-initiated)

3.5.3.1 Device/host expected behavior

See Section 8.1 of Serial ATA Revision 3.5.

The product exit latency (i.e., COMWAKE response) from the slumber state shall start within 10 ms of COMWAKE receipt from the initiator of the wake sequence.

A method for testing the exit latency of a device is for host software to initiate a COMWAKE on the interface. After initiating the request, the host would record the time until the W bit is set to one within the DIAG field of the SError register.

3.5.3.2 Measurement requirements (Device)

The required measurements are:

1) setup bus analyzer (or scope) for tracing of bus activity & begin tracing;
2) if Word 76 bit 9 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one, then proceed to step 3;
3) issue PMREQ_S and receive device response;
4) issue COMWAKE and wait for complete wake of device;
5) issue IDENTIFY DEVICE or IDENTIFY PACKET DEVICE; and
6) repeat the above 10 times.

3.5.3.3 Pass/fail criteria (Device)

The pass/fail requirements are:

1) confirm Slumber wake sequence completion and COMWAKE timing of being within 10 ms of COMWAKE receipt from host (use trace to analyze timings); and
2) the device shall process the command correctly after the complete wake of the device.

3.5.3.4 Measurement requirements (Host)

The required measurements are:

1) setup bus analyzer (or scope) for tracing of bus activity and begin tracing;
2) wait for a Slumber IPM request from the host;

NOTE 17 - There is no guaranteed method for causing the host to send a request. A common ATA (or vendor specific) method which may cause a request from the host is to leave the system idle (up to 10 s).
NOTE 18 - Ensure there is no conflict with a device initiated request.
NOTE 19 - A host vendor may provide a vendor unique tool for initiating the power management requests as to ensure the test does complete as necessary.

3) issue COMWAKE and wait for complete wake of host; and
4) repeat the above 10 times.

3.5.3.5 Pass/fail criteria (Host)

The pass/fail requirements are:

1) confirm Slumber wake sequence completion and ALIGNp of being within 10 ms of COMWAKE receipt from device/emulator/tool (use trace to analyze timings); and

NOTE 20 - In the case that no host initiated request was completed, the pass/fail result shall be na.

2) the worst-case result out of 10 cases shall be reported (i.e., largest value).

3.5.4 IPM-03 : Speed matching upon resume (host-initiated)

3.5.4.1 Device/host expected behavior

See Section 13.2.3.16 of Serial ATA Revision 3.5.

The product signaling speed upon returning from a partial or slumber state shall match the speed prior to entering the partial or slumber state. If a device or host claims support for multiple Serial ATA signaling speeds, then the speed matching upon resume should be applied to all the signaling speeds that the device or host supports.

3.5.4.2 Measurement requirements (Device)

The required measurements are:

1) if Word 76 bit 9 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one, then proceed to step 2, otherwise stop since this test is na;
2) get the current interface rate;

NOTE 21- Determination of the current interface rate is MOI specific.

3) issue PMREQ_P or PMREQ_S and receive device response;
4) issue COMWAKE and wait for complete wake of device;
5) verify the current interface rate; and

NOTE 22 - This requirement shall be verified on 10 total sequences of PMREQ_P if supported and 10 total sequences of PMREQ_S if supported for the current signaling speed established.

6) if the device supports multiple Serial ATA signaling speeds, repeat the above test for all the signaling speeds that the device supports and are established successfully.

NOTE 23 – The method for establishing the different signaling speeds is MOI specific.

3.5.4.3 Pass/fail criteria (Device)

The pass/fail requirements are:

1) a sequence fails if there is no response (i.e., no PMACK or no PMNAK is returned) or if the interface rate changes from before to after the power management sequence;
2) all 10 repetitions shall pass for this test to pass; or
3) if all the sequences result with PMNAKs with no pass or fail sequences, the result is na.

3.5.4.4 Measurement requirements (Host)

The required measurements are:

1) wait for a PMREQ_P or PMREQ_S from the host;

   NOTE 24 – There is no guaranteed method for causing the host to send a request. A common ATA (or vendor specific) method which may cause a request from the host is to leave the system idle and monitor for an appropriate PMREQ for 10 s.
   NOTE 25 – Ensure there is no conflict with a device initiated request.
   NOTE 26 – A host vendor may provide a vendor unique tool for initiating the power management requests as to ensure the test does complete as necessary.

2) issue COMWAKE and wait for complete wake of host;
3) note the current interface rate – determination of the current interface rate is MOI specific;
4) this requirement shall be verified on 10 total sequences of PMREQ_P if supported and 10 total sequences of PMREQ_S if supported for the current signaling speed established; and
5) if the host supports multiple Serial ATA signaling speeds, repeat the above test for all the signaling speeds that the host supports and are established successfully.

3.5.4.5 Pass/fail criteria (Host)

The pass/fail requirements are:

1) a sequence fails if there is no response (i.e., no PMACK or no PMNAK is returned) or if the interface rate changes from before to after the power management sequence;
2) all 10 repetitions shall pass for this test to pass; or
3) if all the sequences result with PMNAKs with no pass or fail sequences, the result is na.

3.5.5 IPM-04 : NAK of requests when support not indicated

3.5.5.1 Device/host expected behavior

See Section 9.7.5 of Serial ATA Revision 3.5.

If a device does not support host interface power management (Word 76 bit 9 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data), upon receipt of a PMREQ_P or PMREQ_S the device should respond with a PMNAK.

If a host does not support device interface power management, upon receipt of a PMREQ_P or PMREQ_S the host should respond with a PMNAK.

3.5.5.2 Measurement requirements (Device)

The required measurements are:

1) if Word 76 bit 9 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is cleared to zero, then proceed to step 2;
2) setup bus analyzer (or scope) for tracing of bus activity & begin tracing;
3) issue PMREQ_P or PMREQ_S and receive device response; and
4) repeat the above 10 times.

3.5.5.3 Pass/fail criteria (Device)

The pass/fail requirements are:

1) if a PMACK is received, then the result is fail, otherwise PMNAK or non-response is a pass; and
2) all 10 repetitions shall pass for this test to pass.

3.5.5.4 Measurement requirements (Host)

The required measurements are:

1) setup bus analyzer (or scope) for tracing of bus activity & begin tracing; and
2) issue PMREQ_P or PMREQ_S and receive host response.

NOTE 27 - This requirement shall be verified on 10 total sequences of PMREQ_P and 10 total sequences of PMREQ_S.

3.5.5.5 Pass/fail criteria (Host)

The pass/fail requirements are:

1) if a PMACK is received, then the result is fail, otherwise PMNAK or non-response is a pass; and
2) all 10 repetitions shall pass for this test to pass.

3.5.6 IPM-05 : Response to PMREQ_P

3.5.6.1 Device/host expected behavior

See Section 9.7.5 of Serial ATA Revision 3.5.

If a device claims support for host-initiated interface power management (Word 76 bit 9 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data), upon receipt of a PMREQ_P the following are valid device responses:

a) respond with a minimum of 4 PMACK primitives and place the device Phy layer into the partial state; or
b) respond with PMNAK until SYNC is received from the host, no device Phy layer power transition shall occur.

If a host claims support for device-initiated interface power management, upon receipt of a PMREQ_P the following are valid host responses:

a) respond with a minimum of 4 PMACK primitives and place the host Phy layer into the partial state; or
b) respond with PMNAK until SYNC is received from the device, no host Phy layer power transition shall occur.

3.5.6.2 Measurement requirements (Device)

The required measurements are:

1) if Word 76 bit 9 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one, then proceed to step 2;
2) setup bus analyzer (or scope) for tracing of bus activity & begin tracing;
3) issue PMREQ_P and receive device response; and
4) repeat the above 10 times.

3.5.6.3 Pass/fail criteria (Device)

The pass/fail requirements are:

1) verify that PMNAK or a minimum of 4 total PMACKs are received (use trace to verify product response); and
2) all 10 repetitions shall pass for this test to pass.

3.5.6.4 Measurement requirements (Host)

The required measurements are:

1) setup bus analyzer (or scope) for tracing of bus activity & begin tracing;
2) issue PMREQ_P and receive host response; and
3) repeat the above 10 times.

3.5.6.5 Pass/fail criteria (Host)

The pass/fail requirements are:

1) verify that PMNAK or a minimum of 4 total PMACKs are received (use trace to verify product response); and
2) all 10 repetitions shall pass for this test to pass.

3.5.7 IPM-06 : Response to PMREQ_S

3.5.7.1 Device/host expected behavior

See Section 9.7.5 of Serial ATA Revision 3.5.

If a device claims support host-initiated interface power management (Word 76 bit 9 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data), upon receipt of a PMREQ_S the following are valid device responses:

a) respond with a minimum of 4 PMACK primitives and place the device Phy layer into the slumber state; or
b) respond with PMNAK until SYNC is received from the host, no device Phy layer power transition shall occur.

If a host claims support for device-initiated interface power management, upon receipt of a PMREQ_S the following are valid host responses:

a) respond with a minimum of 4 PMACK primitives and place the host Phy layer into the slumber state; or
b) respond with PMNAK until SYNC is received from the device, no host Phy layer power transition shall occur.

3.5.7.2 Measurement requirements (Device)

The required measurements are:
1) if Word 76 bit 9 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one, then proceed to step 2;
2) setup bus analyzer (or scope) for tracing of bus activity & begin tracing;
3) issue PMREQ_S and receive device response; and
4) repeat the above 10 times.

3.5.7.3 Pass/fail criteria (Device)

The pass/fail requirements are:
1) verify that PMNAK or a minimum of 4 PMACKs are received (use trace to verify device response); and
2) all 10 repetitions shall pass for this test to pass.

3.5.7.4 Measurement requirements (Host)

The required measurements are:
1) setup bus analyzer (or scope) for tracing of bus activity & begin tracing;
2) issue PMREQ_S and receive device response; and
3) repeat the above 10 times.

3.5.7.5 Pass/fail criteria (Host)

The pass/fail requirements are:
1) verify that PMNAK or a minimum of 4 PMACKs are received (use trace to verify device response); and
2) all 10 repetitions shall pass for this test to pass.

3.5.8 IPM-07 : Device default setting for device initiated requests

3.5.8.1 Device expected behavior

This test is not applicable to hosts.

See Section 13.7.11.2.20 of Serial ATA Revision 3.5.

If a device claims support for device interface power management (Word 78 bit 3 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data), support for device power management shall be disabled (Word 79 bit 3 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) by default. A device shall not issue Partial/Slumber requests unless this feature has been enabled by the host as a result of a SET FEATURES command.

3.5.8.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one, then continue to the next step, otherwise this test is na;
2) issue SET FEATURES (Sector Count = 03h, Features = 10h) to enable device support for initiating power management;
3) power cycle device;
4) save value of Word 79 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE;
5) if SSP is supported and enabled, and DIPM SSP is supported, the test in this loop stops here;
6) issue SET FEATURES (Sector Count = 03h, Features = 10h) to enable device support for initiating power management;
7) issue COMRESET and complete OOB sequence;
8) save value of Word 79 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE; and
9) repeat the above 10 times.

3.5.8.3 Pass/fail criteria

The pass/fail requirements are:

1) verify that Word 79 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is cleared to zero for the stored value(s) in step 4 and step 8 if step 8 is processed; and
2) all 10 repetitions shall pass for this test to pass.

3.5.9 IPM-08 : Device initiated power management enable / disable

3.5.9.1 Device expected behavior

This test is not applicable to hosts.

See Section 13.7.11.3.4 of Serial ATA Revision 3.5.

Support for device power management shall be disabled (Word 79 bit 3 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) by default. A device shall not issue Partial/Slumber requests unless this feature has been enabled by the host as a result of a SET FEATURES command.

3.5.9.2 Measurement requirements

The required measurements are:

1) power cycle device;
2) if Word 78 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;
3) save Word 79 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE;
4) issue SET FEATURES (Sector Count = 03h, Features = 10h) to enable device support for initiating power management;
5) save Word 79 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE;
6) wait for a PMREQ_P or PMREQ_S from the device;

NOTE 28 – There is no guaranteed method for causing the device to send a request. A common method to cause a request is to leave the device idle for 10 s and wait for PMREQ.
NOTE 29 - If no PMREQ_P or PMREQ_S has been issued, issue a STANDBY IMMEDIATE command to device and wait for 10 s for PMREQ.
NOTE 30 – Ensure there is no conflict with a host initiated request.

NOTE 31 – A device vendor may provide a vendor unique tool for initiating the power management requests as to ensure the test does complete as necessary.

7) issue SET FEATURES (Sector Count = 03h, Features = 90h) to disable device support for initiating power management;
8) save Word 79 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE;
9) verify either a PMREQ_S or PMREQ_P is *not* generated using the following method:
    1) leave the device idle and wait 10 s for PMREQ; and
    2) if no PMREQ_P or no PMREQ_S has been issued, issue a STANDBY IMMEDIATE command to device and wait for 10 s for PMREQ;

    and
10) repeat the above 10 times.

3.5.9.3 Pass/fail criteria

The pass/fail requirements are:

1) verify the value of 79 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE saved for the steps above are correct:
    a) step 3 equals cleared to zero;
    b) step 5 equals set to one; and
    c) step 8 equals cleared to zero;

    and

    NOTE 32 - If no device initiated request was completed for any of the test cases when the feature is enabled, the pass/fail result shall be na.

2) all 10 repetitions shall pass for this test to pass.

3.5.10 IPM-09 : Partial state exit latency (device-initiated)

3.5.10.1 Device/host expected behavior

See Section 13.7.11.2.19 of Serial ATA Revision 3.5.

The device and host exit latency (i.e., COMWAKE response) from the partial state shall start within 10 us of COMWAKE receipt from the host.

3.5.10.2 Measurement requirements (Device)

The required measurements are:

1) setup bus analyzer (or scope) for tracing of bus activity & begin tracing;
2) if Word 78 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;
3) wait for a Partial IPM request from the device;

    NOTE 33 - There is no guaranteed method for causing the device to send a request, however a possible method to cause a request is to leave the device idle and wait up to 10 s for a Slumber IPM request. If no Partial IPM request is generated, issue a STANDBY IMMEDIATE command to device and wait up to 10 s.
    NOTE 34 - A device vendor may provide a vendor unique tool for initiating the power management requests as to ensure the test does complete as necessary.

4) issue COMWAKE and wait for complete wake of device;
5) issue IDENTIFY DEVICE or IDENTIFY PACKET DEVICE; and
6) this requirement shall be verified on 10 total sequences.

3.5.10.3 Pass/fail criteria (Device)

The pass/fail requirements are:

1) confirm partial wake sequence completion and host transmission of ALIGNp within 10 us of COMWAKE receipt from device/emulator/tool (use trace to analyze timings);

NOTE 35 - If no device initiated request was completed for any of the test sequences, the pass/fail result shall be na.

2) the device shall process the command correctly after the complete wake of the device; and
3) all 10 repetitions shall pass for this test to pass.

3.5.10.4 Measurement requirements (Host)

The required measurements are:
1) setup bus analyzer (or scope) for tracing of bus activity and begin tracing;
2) issue PMREQ_P to host;
3) issue COMWAKE and wait for complete wake of host; and
4) this requirement shall be verified on 10 total sequences.

3.5.10.5 Pass/fail criteria (Host)

The pass/fail requirements are:
1) confirm partial wake sequence completion and host transmission of ALIGNp within 10 us of COMWAKE receipt from device/emulator/tool (use trace to analyze timings);

NOTE 36 - In the case that no host initiated-request was completed, the pass/fail result shall be na.

2) the worst-case time out of 10 repetitions shall be reported (i.e., largest value); and
3) all 10 repetitions shall pass for this test to pass.

3.5.11 IPM-10 : Slumber state exit latency (device-initiated)

3.5.11.1 Device/host expected behavior

See Section 13.7.11.2.19 of Serial ATA Revision 3.5.

The product exit latency (i.e., COMWAKE response) from the slumber state shall start within 10 ms of COMWAKE receipt from the host.

A method for testing the exit latency of a device is for host software to initiate a COMWAKE on the interface. After initiating the request, the host would record the time until the W bit is set to one within the DIAG field of the SError register.

3.5.11.2 Measurement requirements (Device)

The required measurements are:
1) setup bus analyzer (or scope) for tracing of bus activity & begin tracing;
2) if Word 78 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;
3) wait for a Slumber IPM request from the device;

NOTE 36 – There is no guaranteed method for causing the device to send a request, however a possible method to cause a request is to leave the device idle and wait up to 10 s for a Slumber IPM request. If no Partial IPM request is generated, issue a STANDBY IMMEDIATE command to device and wait up to 10 s.
NOTE 378 - A device vendor may provide a vendor unique tool for initiating the power management requests as to ensure the test does complete as necessary.

4) issue COMWAKE and wait for complete wake of device;
5) issue IDENTIFY DEVICE or IDENTIFY PACKET DEVICE; and
6) this requirement shall be verified on 10 total sequences.

3.5.11.3 Pass/fail criteria (Device)

The pass/fail requirements are:
1) confirm Slumber wake sequence completion and COMWAKE timing of being within 10 ms of COMWAKE receipt from host (use trace to analyze timings);

2) if no device-initiated request was completed for any of the test sequences, the pass/fail result shall be na;
3) the device shall process the command correctly after the complete wake of the device; and
4) all 10 repetitions shall pass for this test to pass.

3.5.11.4 Measurement requirements (Host)

The required measurements are:
1) setup bus analyzer (or scope) for tracing of bus activity & begin tracing;
2) issue PMREQ_S to host;
3) issue COMWAKE and wait for complete wake of host; and
4) repeat this test 10 times.

3.5.11.5 Pass/fail criteria (Host)

1) confirm partial wake sequence completion and host transmission of ALIGNp within 10 us of COMWAKE receipt from device/emulator/tool (use trace to analyze timings);

   NOTE 39 - In the case that no host-initiated request was completed, the pass/fail result shall be na.

2) the worst-case time out of 10 repetitions shall be reported (i.e., largest value); and
3) all 10 repetitions shall pass for this test to pass.

3.5.12 IPM-11 : Speed matching upon resume (device-initiated)

3.5.12.1 Device/host expected behavior

See Section 13.7.11.2.19 of Serial ATA Revision 3.5.

The product signaling speed upon returning from a partial or slumber state shall match the speed prior to entering the partial or slumber state.

If a device or host claims support for multiple Serial ATA signaling speeds, then the speed matching upon resume should be applied to all the signaling speeds that the device or host supports.

3.5.12.2 Measurement requirements (Device)

The required measurements are:
1) if Word 78 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;
2) get the current interface rate;

   NOTE 40 - Determination of the current interface rate is MOI specific.

3) wait for an IPM request from the device;

   NOTE 41 - There is no guaranteed method for causing the device to send a request, however a possible method to cause a request is to leave the device idle and wait up to 10 s for a Slumber IPM request. If no Partial IPM request is generated, issue a STANDBY IMMEDIATE command to device and wait up to 10 s.
   NOTE 42 - A device vendor may provide a vendor unique tool for initiating the power management requests as to ensure the test does complete as necessary.

5) issue COMWAKE and wait for complete wake of device;
6) verify the current interface rate;
7) this requirement shall be verified on 10 total sequences of PMREQ_P if supported and 10 total sequences of PMREQ_S if supported for the current signaling speed established; and
8) if the device supports multiple Serial ATA signaling speeds, repeat the above test for all the signaling speeds that the device supports and are established successfully.

   NOTE 43 - How to establish the different signaling speed is MOI specific.

3.5.12.3 Pass/fail criteria (Device)

The pass/fail requirements are:

1) a sequence fails if there is no response (i.e., no PMACK or no PMNAK is returned) or if the interface rate changes from before to after the power management sequence;
2) if one or more of the sequences fails, the test result is fail; or
3) if all the sequences result with PMNAKs and no pass or fail sequences, the result is na.

3.5.12.4 Measurement requirements (Host)

The required measurements are:

1) issue PMREQ_P or PMREQ_S and receive host response;
2) issue COMWAKE and wait for complete wake of host;
3) save the value of the current interface rate;

   NOTE 44 - Determination of the current interface rate is MOI specific.

4) this requirement shall be verified on 10 total sequences of PMREQ_P, if supported and 10 total sequences of PMREQ_S, if supported for the current signaling speed established; and
5) if the host supports multiple Serial ATA signaling speeds, repeat the above test for all the signaling speeds that the host supports and are established successfully.

   NOTE 45 - How to establish the different signaling speed is MOI specific.

3.5.12.5 Pass/fail criteria (Host)

The pass/fail requirements are:

1) a sequence fails if there is no response (i.e., no PMACK or no PMNAK is returned) or if the interface rate changes from before to after the power management sequence;
2) if one or more of the sequences fails, the test result is fail; or
3) if all the sequences result with PMNAKs and no pass or fail sequences, the result is na.

3.5.13 IPM-12 : IPM is mandatory

3.5.13.1 Device expected behavior

See 13.7.10.2.5, 13.7.10.2.18, and 13.7.10.2.19 of Serial ATA Revision 3.5.

If the device supports Serial ATA Revision 3.1 or above, IPM is required.

3.5.13.2 Measurement requirements

The required measurements are:

1) if Word 222 bit 6 or above (up to bit 11) is set to one, then continue to the next step, otherwise stop since this test is na;
2) save value of Word 76 Bit 9; and
3) save value of Word 78 Bit 3.

3.5.13.3 Pass/fail criteria

The pass/fail requirements are:

1) verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE has at least one of Word 76 Bit 9 or Word 78 bit 3 set to one.

3.6 Digital optional features

3.6.1 DOF-01 : Asynchronous notification

3.6.1.1 Device expected behavior

This test is not applicable to ATA devices and hosts nor is it applicable to devices without manual eject capabilities.

See Section 13.10 of Serial ATA Revision 3.5.

Asynchronous notification is a mechanism for a device to send a notification to the host that the device requires attention. The device shall have the Asynchronous Notification feature enabled by the host before the device may set the N bit to one in the Set Device Bits FIS.

3.6.1.2 Measurement requirements

The required measurements are:

1) if the device has an Eject button, then continue to the next step, otherwise stop since this test is na;
2) power cycle device;
3) save value of Word 78 bit 5 in IDENTIFY PACKET;
4) save Word 79 bit 5 in IDENTIFY PACKET DEVICE;
5) issue SET FEATURES (Sector Count = 05h, Features = 10h) to enable device support for Asynchronous Notification;
6) save Word 79 bit 5 in IDENTIFY PACKET DEVICE;
7) manually press Eject button on the ATAPI device to let the tray or the media out;
8) record status or receipt of Set Devices Bits FIS with the Interrupt 'I' bit set to one and the Notification "N" bit set to one;
9) issue Get Event/Status Notification command to acknowledge the notification;
10) manually push in the media or the tray or press Eject button on the ATAPI device to let the tray in;
11) record status of receipt of Set Devices Bits FIS with the Interrupt 'I' bit set to one and the Notification "N" bit set to one;
12) issue Get Event/Status Notification command to acknowledge the notification;
13) issue SET FEATURES (Sector Count = 05h, Features = 90h) to disable device support for Asynchronous Notification;
14) save value of Word 79 bit 5 in IDENTIFY PACKET DEVICE;
15) manually press Eject button on the ATAPI device to let the tray or the media out;
16) record absence of Devices Bits FIS;
17) manually push in the media or the tray or press Eject button on the ATAPI device to let the tray in;
18) record absence of Devices Bits FIS; and
19) this requirement shall be verified on 5 total sequences.

3.6.1.3 Pass/fail criteria

The pass/fail requirements are:

1) verify Word 78 bit 5 is set to one in step 3 above;
2) verify Word 79 bit 5 is set to one in step 4 above;
3) verify Word 79 bit 5 is cleared to zero in step 6 above;
4) verify Set Device Bits FIS received correctly when this feature is enabled in step 8 above;
5) verify Set Device Bits FIS received correctly when this feature is enabled in step 11 above;
6) verify Word 79 bit 5 is cleared to zero in step 14 above;
7) verify Set Device Bits FIS is not received in step 17; and
8) verify Set Device Bits FIS is not received in step 19.

3.6.2 DOF-02 : Phy speed indicator

3.6.2.1 Device expected behavior

This test is not applicable to hosts.

See Section 13.7.11.3 of Serial ATA Revision 3.5.

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Support for Phy speed indicator is optional and if not supported, Word 77 bits 3:1 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE shall be cleared to zero indicating the device has no support for this feature.

If a device claims support for multiple Serial ATA signaling speeds, then Phy speed indicator if supported should be applied to all the signaling speeds that the device supports.

3.6.2.2 Measurement requirements

The required measurements are:

1) get the current interface rate;

   NOTE 46 - Determination of the current interface rate is MOI specific.

2) save the values of Word 77 bits 3:1 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE; and
3) if the device supports multiple Serial ATA signaling speeds, then repeat the above test for all the signaling speeds that the device supports which are established successfully.

   NOTE 47 - How to establish the different signaling speed is MOI specific.

3.6.2.3 Pass/fail criteria

The pass/fail requirements are:

1) if WORD 77 bits 3:1 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE are always cleared to zero for all the signaling speeds that the device supports which are established successfully, then this feature is not supported and the result is na; and
2) otherwise, verify the values saved in step 2 are set correctly when the corresponding speed is supported and established successfully. They shall be equal to the interface rate (e.g., for Gen-1, the value of WORD bits 3:1 shall be equal to one, for Gen2, the value of WORD 77 bits 3:1 shall be equal to two, and so on).

3.7 Device Sleep

3.7.1 Overview

The Device Sleep (SLP) test requirements are determined by the requirements of the feature as defined in Serial ATA Revision 3.5.

Most of the tests listed in this section require that support for Device Sleep is claimed by the product for verification of the expected behavior. Support for Device Sleep is verified by reading Word 78 bit 8 set to one in IDENTIFY DEVICE data.

3.7.2 SLP-01: Identify Device Data log support

3.7.2.1 Device expected behavior

See Section 8.5.3 of Serial ATA Revision 3.5.

Devices that support Device Sleep shall support the Identify Device Data log, and the DEVSLP TIMING VARIABLES SUPPORTED bit shall be set to one, and the POWER DISABLE FEATURE ALWAYS ENABLED bit shall be cleared to zero.

3.7.2.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 8 in IDENTIFY DEVICE is set to one (Device Sleep supported), then continue to the next step, otherwise stop since the result for this test is not required;
2) issue and complete an IDENTIFY DEVICE command;
3) issue and complete a READ LOG EXT command with Log Address 00h;
4) issue and complete a READ LOG EXT command with Log Address 30h, page 00h; and
5) issue and complete a READ LOG EXT command with Log Address 30h, page 08h.

3.7.2.3 Pass/fail criteria

The pass/fail requirements are:

1) verify Word 87 Bit 5 is set to one in step 2 above;
2) verify the number of Log pages at Log Address 30h is larger than 1;

3) verify that Page 08h in Log Address 30h is supported;
4) verify the DEVSLP TIMING VARIABLES SUPPORTED bit (Qword 6 bit 63) is set to one; and
5) verify the POWER DISABLE FEATURE ALWAYS ENABLED bit (Qword 1 bit 31) is cleared to zero.

3.7.3 SLP-02: Default setting for Device Sleep

3.7.3.1 Device expected behavior

See Section 8.5.3 of Serial ATA Revision 3.5.

The Device Sleep feature shall be disabled as a result of processing a power on reset.

3.7.3.2 Measurement requirements

The required measurements are:
1) if Word 78 bit 8 in IDENTIFY DEVICE is set to one (Device Sleep supported), then continue to the next step, otherwise stop since the result for this test is not required;
2) issue and complete a SET FEATURE command with Sector Count = 09h, Features = 10h;
3) power on reset the device;
4) issue and complete an IDENTIFY DEVICE command;
5) issue and complete a READ LOG EXT command with Log Address 30h, Page 08h;
6) if SSP is supported and enabled, test stops here;
7) issue and complete a SET FEATURE command with Sector Count = 09h, Features = 10h;
8) send a COMRESET and complete the OOB sequence;
9) issue and complete an IDENTIFY DEVICE command;
10) issue and complete a READ LOG EXT command with Log Address 30h, Page 08h; and
11) repeat the above 10 times.

3.7.3.3 Pass/fail criteria

The pass/fail requirements are:
1) verify Word 79 bit 8 in IDENTIFY DEVICE is cleared to zero after the power on reset;
2) verify Qword 2 bit 10 in the Identify Device Data log is cleared after the power on reset;
3) verify Word 79 bit 8 in IDENTIFY DEVICE is cleared after the COMRESET;
4) verify Qword 2 bit 10 in the Identify Device Data log is cleared after the COMRESET; and
5) all 10 repetitions must pass for this test to pass.

3.7.4 SLP-03: Device Sleep Enable/Disable states

3.7.4.1 Device expected behavior

See Section 8.5.2 of Serial ATA Revision 3.5.

The state of device sleep feature shall be reflected in the Identify Device and Identify Device Data log.

3.7.4.2 Measurement requirements

The required measurements are:
1) if Word 78 bit 8 in IDENTIFY DEVICE is set to one, then continue to the next step, otherwise stop since this test is na;
2) issue SET FEATURES (Sector Count = 09h, Features = 10h) to enable device sleep;
3) save value of Word 79 bit 8 in IDENTIFY DEVICE and Qword 2 Bit 10 in Identify Device Data log, Page 08h;
4) issue SET FEATURES (Sector Count = 09h, Features = 90h) to disable device sleep;
5) save value of Word 79 bit 8 in IDENTIFY DEVICE and Qword 2 Bit 10 in Identify Device Data log, Page 08h.

3.7.4.3 Pass/fail criteria

The pass/fail requirements are:
1) verify Word 79 bit 8 in IDENTIFY DEVICE is set to one in step 3;

2) verify Qword 2 bit 10 in the Identify Device Data log, page 08h is set to one in step 3;
3) verify Word 79 bit 8 in IDENTIFY DEVICE is cleared in step 5; and
4) verify Qword 2 bit 10 in the Identify Device Data log, page 08h is cleared to zero in step 5.

3.7.5 SLP-04: Lack of Device Sleep support

3.7.5.1 Device expected behavior

See Section 8.5.2 of Serial ATA Revision 3.5.

If a device does not support Device Sleep (Word 78 bit 8 cleared to zero in IDENTIFY DEVICE), Set Features to enable Device Sleep shall return command abort.

3.7.5.2 Measurement requirements

The required measurements are:
1) if Word 78 bit 8 in IDENTIFY DEVICE is cleared to zero (Device Sleep not supported), then continue to the next step, otherwise stop since the result for this test is not required;
2) issue and complete a SET FEATURE command with Sector Count = 09h, Features = 10h; and
3) issue and complete an IDENTIFY DEVICE command.

3.7.5.3 Pass/fail criteria

The pass/fail requirements are:
1) verify the SET FEATURE command is aborted; and
2) verify Word 79 bit 8 in IDENTIFY DEVICE is cleared to zero.

3.7.6 SLP-05: Info Consistency between IDENTIFY DEVICE and Identify Device Data log

3.7.6.1 Device expected behavior

See Sections 8.5.2 and 13.7.11 of Serial ATA Revision 3.5.

The state of device sleep feature shall be reflected in the Identify Device and Identify Device Data log.

3.7.6.2 Measurement requirements

The required measurements are:
1) if Word 78 bit 8 in IDENTIFY DEVICE is set to one (Device Sleep supported), then continue to the next step otherwise stop since the result for this test is not required;
2) issue and complete an IDENTIFY DEVICE command; and
3) issue and complete a READ LOG EXT command with Log Address 30h, Page 08h.

3.7.6.3 Pass/fail criteria

The pass/fail requirements are:
1) verify Word 78 Bit 8 (DEVICE SLEEP SUPPORTED) of Identify device is identical to Qword 1 bit 25 of Identify Device Data log, Page 08h;
2) verify Word 79 bit 8 (DEVICE SLEEP ENABLED) of Identify device is identical to Qword 2 bit 10 of Identify Device Data log, Page 08h;
3) verify Word 77 bit 7 (DEVSLEEP_TO_REDUCEDPWRSTATE CAPABILITY SUPPORTED) of Identify device is identical to Qword 1 bit 26 of Identify Device Data log, Page 08h; and
4) verify Word 77 bit 8 (POWER DISABLE FEATURE ALWAYS ENABLED) in DEVICE IDENTIFY is identical to Qword 1 bit 31 in Identify Device Data log, Page 08h.

3.7.7 SLP-06: Device Sleep invoked from Active state

3.7.7.1 Device expected behavior

See Section 8.5 of Serial ATA Revision 3.5.

If a device supports Device Sleep, it can enter the Device Sleep state from the Active state.

After asserting DEVSLP, the device shall enter the DevSleep interface power state; the device shall not initiate any device to host communications; and the device shall ignore any host to device communications.

3.7.7.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 8 in IDENTIFY DEVICE is set to one (Device Sleep supported), then continue to the next step, otherwise stop since the result for this test is not required;
2) issue and complete a SET FEATURE command with Sector Count = 09h, Features = 10h;
3) issue and complete an IDENTIFY DEVICE command;
4) assert DEVSLP;
5) wait at least 1 s (DXET, per Tech proposal 80); and
6) send COMRESET.

3.7.7.3 Pass/fail criteria

The pass/fail requirements are:

1) verify the device has not initiated any device to host communications; and
2) verify the device has not responded with COMINIT to the COMRESET in step 6.

3.7.8 SLP-07: Device Sleep invoked from Partial state

3.7.8.1 Device expected behavior

See Section 8.5 of Serial ATA Revision 3.5.

If a device supports Device Sleep, it can enter the Device Sleep state from the Partial state.
After asserting DEVSLP, the device shall enter the DevSleep interface power state; the device shall not initiate any device to host communications; and the device shall ignore any host to device communications.

3.7.8.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 8 in IDENTIFY DEVICE is set to one (Device Sleep supported), then continue to the next step, otherwise stop since the result for this test is not required;
2) issue and complete a SET FEATURE command with Sector Count = 09h, Features = 10h;
3) issue and complete an IDENTIFY DEVICE command;
4) invoke the SATA interface into Partial state. If the device supports HIPM, invoke Partial state via HIPM, otherwise try DIPM;
5) if the device is in the expected state, continue to the next step, otherwise the test is na;
6) assert DEVSLP;
7) wait at least 1 s (DXET, per Tech proposal 80); and
8) send COMRESET.

3.7.8.3 Pass/fail criteria

The pass/fail requirements are:

1) verify the device has not initiated any device to host communications; and
2) verify the device has not responded with COMINIT to the COMRESET in step 8.

3.7.9 SLP-08: Device Sleep invoked from Slumber state

3.7.9.1 Device expected behavior

See Section 8.5 of Serial ATA Revision 3.5.

If a device supports Device Sleep, it can enter the Device Sleep state from the Slumber state.
After asserting DEVSLP, the device shall enter the DevSleep interface power state; the device shall not initiate any device to host communications; and the device shall ignore any host to device communications.

3.7.9.2 Measurement requirements

The required measurements are:

1) if Word 78 bit 8 in IDENTIFY DEVICE is set to one (Device Sleep supported), then continue to the next step, otherwise stop since the result for this test is not required;
2) issue and complete a SET FEATURE command with Sector Count = 09h, Features = 10h;
3) issue and complete an IDENTIFY DEVICE command;
4) invoke the SATA interface into Slumber state. If the device supports HIPM, invoke Slumber state via HIPM, otherwise try DIPM;
5) if the device is in the expected state, continue the next step, otherwise, the test is na;
6) assert DEVSLP;
7) wait at least 1 s; and
8) send COMRESET.

3.7.9.3 Pass/fail criteria

The pass/fail requirements are:

1) verify the device has not initiated any device to host communications; and
2) verify the device has not responded with COMINIT to the COMRESET in step 8.

3.7.10 SLP-09: DevSleep interface power state exit timing

3.7.10.1 Device/Host expected behavior

See Section 8.5.1 of Serial ATA Revision 3.5.

The device shall be ready to detect OOB signals in less than or equal to 20 ms or DETO field (defined in Identify Device Data log) after Negating DEVSLP.

3.7.10.2 Measurement requirements (Device)

The required measurements are:

1) if Word 78 bit 8 IDENTIFY DEVICE is set to one, then continue to the next step, otherwise stop since the result for this test is not required;
2) issue SET FEATURES (Sector Count = 09h, Features = 10h);
3) assert DEVSLP;
4) wait at least 1 s (DXET, per Tech proposal 80);
5) Send COMRESET;
6) de-assert DEVSLP;
7) wait at least 20 ms if DETO is cleared to zero or if DETO field (defined in Identify Device Data log) is not cleared to zero after Negating DEVSLP; and
8) send COMRESET.

3.7.10.3 Pass/fail criteria

The pass/fail requirements are:

1) verify the device has not initiated any device to host communications;
2) verify the device has not responded with COMINIT to the COMRESET in step 5; and
3) verify the device has exited Device Sleep state by responding with COMINIT and progressing to reconnect with the Host after the second COMRESET sent by the test station in step 8.

3.7.10.4 Measurement requirements (Host)

The required measurements are:

1) setup bus analyzer (or scope) for tracing of bus activity and begin tracing;
2) assert DEVSLP;
3) wait at least 1 s (DXET, per Tech proposal 80);
4) power off device;
5) wait 10 s;
6) power on device; and
7) repeat the above 10 times.

3.7.10.5 3.7.10.5 Pass/fail criteria (Host)

The pass/fail requirements are:

1) verify that in step 2 above the interface is in DevSleep power management state with the value of the HBA SStatus register set to 8xxh.
2) verify that in step6 above device issues COMINIT and the host does not respond to device COMINIT with COMRESET, and the value of the HBA SStatus register remains as 8xxh; and
3) all 10 repetitions shall pass for this test to pass.

3.7.11 SLP-10: Host DevSleep interface power state exit

3.7.11.1 Host expected behavior

See Section 8.5.1 of Serial ATA Revision 3.5.

The host shall be ready to exit the DevSleep when the DEVSLP signal is removed and issue COMRESET to establish the Active SATA bus.

3.7.11.2 Measurement requirements (Host)

The required measurements are:

1) setup bus analyzer (or scope) for tracing of bus activity and begin tracing;
2) assert DEVSLP;
3) wait at least 1 s (DXET, per Tech proposal 80);
4) power off device;
5) wait 10 s;
6) power on device;
7) wait 1 s;
8) de-assert DEVSLP;
9) wait 1 s;
10) assert DEVSLP;
11) wait 1 s;
12) de-assert DEVSLP; and
13) repeat the above 10 times.

3.7.11.3 Pass/fail criteria (Host)

The pass/fail requirements are:

1) observe that in step 9 above the host responds to device COMINIT with COMRESET and that the interface has transitioned to Active state with the value of the HBA SStatus register set to 1xxh.
2) observe that in step 11 above the interface is in DevSleep power management state with the value of the HBA SStatus register set to 8xxh.
3) observe that in step 12 above the interface is in Active state with the value of the HBA SStatus register set to 1xxh; and
4) all 10 repetitions shall pass for this test to pass.

3.8 Mechanical - cable assembly - standard internal and eSATA

3.8.1 Overview

If both ends of a cable have identical connector types, then the mechanical tests shall only need to be verified on one end of the cable.

The tester shall ensure that the cable assemblies are clearly labeled so that each line in a cable assembly is able to be uniquely identified. For a standard internal cable assembly, a suggested labeling method is:

a) each of the cables is labeled;
b) the two ends of the cable are also labeled (e.g., Recept_A, Recept_B); and
c) the signal lines use the pin names provided in the Specification. For standard internal connectors Table 5 and Figure 34 of Section 6.2.3.2, in the Serial ATA Revision 3.5 labels the individual

signal lines as S1, S2, S3, …S6, S7. It also defines Pair A as being the combination of signal lines S2 and S3, while Pair B is defined as the combination of signal lines S5 and S6.

If a family of cables is being tested, all tests shall be performed on only one of the cables (longest or shortest).

To ensure that tests are processed in an order to minimize impact between results gathered for the different tests, the following considerations are necessary for executing the mechanical cable tests:

a) all SI (electrical tests) shall be completed on a cable sample prior to any mechanical tests;
b) for internal SATA cables, the cable sample used to verify MCI-02, MCI-03, MCI-04 shall be a different physical sample from which is used to verify MCI-01 and MCX-05; and
c) for eSATA cables the samples used for MCE-01 and MCX-05 shall be the same sample.

3.8.2 MCI-01 : Visual and dimensional inspections

3.8.2.1 Cable assembly expected behavior

See Section 6.2.4, Figure 35 and Figure 36 of the Serial ATA Revision 3.5.

3.8.2.2 Measurement requirements

This test is only applicable to standard internal (latching and non-latching) SATA cables.

The required measurements are:

a) the height of the slot (for the device plug tongue) shall be 1.40 mm ± 0.08 mm (see Serial ATA Revision 3.5 Figure 35, section A-A);
b) the width of the slot (for the device plug tongue) shall be 10.57 mm ± 0.08 mm (see Serial ATA Revision 3.5 Figure 35);
c) the height of the slot for the device plug key shall be 2.40 mm ± 0.08 mm (see Serial ATA Revision 3.5 Figure 35);
d) the width of the slot for the device plug key shall be 1.31 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 35);
e) for a non-latching cable the width of the cable retention feature (bump) shall be 1.50 mm ± 0.20 mm (see Serial ATA Revision 3.5 Figure 32);
f) for a latching cable there shall be no cable retention feature (bump), as shown in Serial ATA Revision 3.5 Figure 36;
g) for a latching cable the distance from the slot to the top surface of the receptacle shall be 1.45 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 36); and
h) for a latching cable the latch engagement feature shall be able to deflect below 1.50 mm (see Serial ATA Revision 3.5 Figure 36).

3.8.2.3 Pass/fail criteria

All applicable measurements within this test shall be verified as a pass for this test pass.

3.8.3 MCI-02 : Insertion force (latching and non-Latching)

3.8.3.1 Cable assembly expected behavior

See Section 6.2.10.3, Table 8 of the Serial ATA Revision 3.5.

3.8.3.2 Measurement requirements

This test is only applicable to standard internal (latching and non-latching) SATA cables.

For Serial ATA Interoperability Program testing a total of 20 insertion/removal force cycles shall be used for this measurement.

3.8.3.3 Pass/fail criteria

The maximum limit is 45 N.

3.8.4 MCI-03 : Removal force (non-latching)

3.8.4.1 Cable assembly expected behavior

See Section 6.2.10.3, Table 8 of the Serial ATA Revision 3.5.

3.8.4.2 Measurement requirements

This test is only applicable to standard non-latching internal SATA cables.

For Serial ATA Interoperability Program testing a total of 20 insertion/removal force cycles shall be used for this measurement.

3.8.4.3 Pass/fail criteria

Minimum limit is 10 N through 20 cycles

3.8.5 MCI-04 : Removal force (latching)

3.8.5.1 Cable assembly expected behavior

See Section 6.2.10.3, Table 8 of the Serial ATA Revision 3.5.

3.8.5.2 Measurement requirements

This test is only applicable to standard latching internal SATA cables.

A total of 20 insertion/removal force cycles shall be used for this measurement.

3.8.5.3 Pass/fail criteria

No damage and no disconnect with 25 N static load applied after 20 mating cycles.

3.8.6 MCI-05 : Cable pull-out - internal (normative) and eSATA (informative) cables

3.8.6.1 Cable assembly expected behavior

See Section 6.2.10.3, Table 8 of the Serial ATA Revision 3.5.

3.8.6.2 Measurement requirements

This test is applicable to standard internal (latching and non-latching) SATA and eSATA cables.

The required measurements are:

1) exert a 40 N static load to a cable for at least 1 minute to ensure the wire-to-connector junction will not fail; and
2) a before and after test resistance measurement shall be made and the difference shall be the change in resistance.

3.8.6.3 Pass/fail criteria

The pass/fail requirements are:

1) all applicable measurements within this test shall be verified for this test requirement to pass;
2) no visible physical damage; and
3) the change in resistance shall not be greater than 1.0 ohm.

3.8.7 MCE-01 : Visual and dimension inspection for eSATA cables (informative)

3.8.7.1 Expected behavior

See overview and references to Serial ATA Revision 3.5.

3.8.7.2 Measurement requirements

The required measurements are:

a) insertion and Removal forces (qualitative check only):
    a) insertion of cable receptacle connector into the device/host plug connector should be with ease. If excessive, check insertion force (maximum is 40 N). See Section 6.2.10.3 of the Serial ATA Revision 3.5; and
    b) removal of cable receptacle connector from the device/host plug connector should have no evidence of weakness (reference is a minimum 10 N). As alternate to force test, verify the true positions of the retention features (rectangular holes x4) per pass/fail criteria. These holes shall mate properly with the retention spring x4 of the plug connector;
b) the height of the slot (for plug tongue) shall be 1.40 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 143);
c) the thickness of the left key shall be 1.30 mm ± 0.08 mm (see Serial ATA Revision 3.5 Figure 143);
d) the thickness of the right key shall be 1.30 mm ± 0.08 mm (see Serial ATA Revision 3.5 Figure 143);
e) the height of receptacle shall be 3.80 mm ± 0.1 mm (see Serial ATA Revision 3.5 Figure 143);
f) the distance between outermost latching springs shall be 4.30 mm ± 0.1 mm (see Serial ATA Revision 3.5 Figure 143);
g) the width of the slot (for plug tongue) shall be 10.15 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 143);
h) the width of the top wall shall be 9.50 mm ± 0.10 mm (see Serial ATA Revision 3.5 Figure 143);
i) the width of the bottom wall shall be 12.70 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 143);
j) the distance between the outermost key sides shall be 14.80 mm ± 0.10 mm (see Serial ATA Revision 3.5 Figure 143);
k) *informative - The optional feature - dimple height shall be 0.25 mm ± 0.05 mm (*see Serial ATA Revision 3.5 *Figure* 143*);*
l) the retention features (1.7 mm by 1.5 mm areas x4) shall be within 4.25 mm ± 0.10 mm to datum (Y) (see Serial ATA Revision 3.5 Figure 143);
m) the retention features (1.7 mm by 1.5 mm areas x4) shall be bilaterally located within 6.8 mm ± 0.1 mm to the connector center axis. (see Serial ATA Revision 3.5 Figure 143); and
n) *informative - The distance of all spring contact points (with the blades of plug connector) shall be 2.90 mm ± 0.15 mm from datum plane Y (*see Serial ATA Revision 3.5 *Figure* 143*).*

3.8.7.3 Pass/fail criteria

All applicable measurements within this test shall be verified for this test requirement to pass.

3.9 Electrical - cable assembly – standard internal and eSATA

3.9.1 Overview

The Serial ATA Specification currently specifies a 20 % to 80 % rise time for the test pulse. However, test equipment rise time filters are usually programmed with 10 % to 90 % values. Thus, some conversion is needed. An example conversion for 70 ps measured from 20 % threshold to 80 % threshold would be to set up the rise time filter for a 105 ps rise time, measured from 10 % threshold to 90 % threshold.
.

The tester shall ensure that the cable assemblies are clearly labeled so that each line in a cable assembly is able to be uniquely identified. For a standard internal cable assembly, a suggested labeling method is:

a) each of the cables is labeled;
b) the two ends of the cable are also labeled (e.g., Recept_A, Recept_B); and
c) the signal lines use the pin names provided in the Specification. For standard internal connectors Table 5 and Figure 34 of Section 6.2.3.2, in the Serial ATA Revision 3.5 labels the individual signal lines as S1, S2, S3, …S6, S7. It also defines Pair A as being the combination of signal lines S2 and S3, while Pair B is defined as the combination of signal lines S5 and S6.

If a family of cables is being tested, then all tests shall be performed on both the longest and shortest lengths unless noted in a specific test.

Tester is required to save all the calibration data (i.e., screen shot) that is done daily at a minimum, if not every cable evaluation. Valid calibration data shall be available per product for review, even if the same calibration data (i.e., daily) is used for multiple products. It is required that calibration be completed for this area of testing to ensure consistent measurements and environment impacts.

3.9.2 SI-01 : Mated connector impedance

3.9.2.1 Cable assembly expected behavior

See Section 6.12.2, Table 36 for internal and Table 37 for eSATA of the Serial ATA Revision 3.5.

3.9.2.2 Measurement requirements

The required measurements are:

a) this test is normative for internal SATA and informative for eSATA cables;
b) the test shall be performed on both ends of the cable assembly, for each differential pair of the assembly; and
c) follow procedure P1 in Table 40 in Section 6.12.3.4 of the Serial ATA Revision 3.5.

3.9.2.3 Pass/fail criteria

Mated Connector Differential Impedance shall be 100 ohm with a relative tolerance of ± 15 %.

3.9.3 SI-02 : Cable absolute impedance

3.9.3.1 Cable assembly expected behavior

See Section 6.12.2, Table 36 for internal and Table 37 for eSATA of the Serial ATA Revision 3.5.

3.9.3.2 Measurement requirements

The required measurements are:

a) this test is normative for internal SATA cables and informative for eSATA cables;
b) follow procedure P2 in Table 40 in Section 6.12.3.4 of the Serial ATA Revision 3.5; and
c) the test shall be performed on one end of the cable assembly, for each differential pair of the assembly.

3.9.3.3 Pass/fail criteria

Cable Absolute Differential Impedance shall be 100 ohm with a relative tolerance of ± 10 %.

3.9.4 SI-03 : Cable pair matching

3.9.4.1 Cable assembly expected behavior

See Section 6.12.3.4, Table 40 of the Serial ATA Revision 3.5.

3.9.4.2 Measurement requirements

The required measurements are:

a) this test is normative for internal SATA cables and informative for eSATA cables;
b) follow procedure P3 in Table 40 in Section 6.12.3.4 of the Serial ATA Revision 3.5; and
c) the test shall be performed on one end of the cable assembly, for each differential pair of the assembly.

3.9.4.3 Pass/fail criteria

Cable Pair Matching Impedance shall be ± 5 ohm.

3.9.5 SI-04 : Common mode impedance

3.9.5.1 Cable assembly expected behavior

See Section 6.12.2, Table 36 for internal and Table 37 for eSATA of the Serial ATA Revision 3.5.

3.9.5.2 Measurement requirements

The required measurements are:

a) this test is normative for internal SATA cables and informative for eSATA cables;
b) follow procedure P4 in Table 40 of Section 6.12.3.4 of the Serial ATA Revision 3.5; and
c) the test shall be performed on one end of the cable assembly, for each differential pair of the assembly.

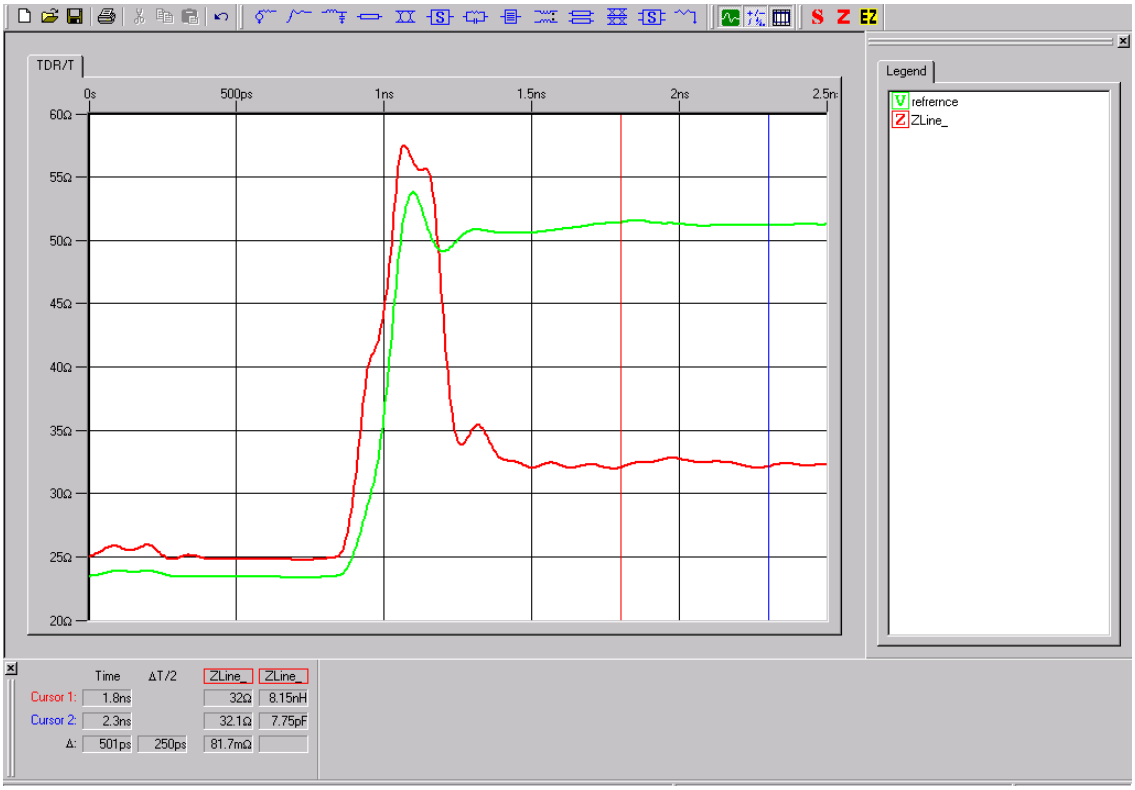


Figure 1 – Example result showing the last vestige of the connector response (at 1.8 ns)

3.9.5.3 Pass/fail criteria

Common Mode Impedance shall be 25 ohm to 40 ohm.

3.9.6 SI-05 : Differential rise time

3.9.6.1 Cable assembly expected behavior

See Section 6.12.2, Table 36 for internal and Table 37 for eSATA of the Serial ATA Revision 3.5.

3.9.6.2 Measurement requirements

The required measurements are:

a) this test is normative for internal SATA cables and informative for eSATA cables; and
b) follow procedure P8 in Table 40 of Section 6.12.3.4 of the Serial ATA Revision 3.5.

3.9.6.3 Pass/fail criteria

The pass/fail requirements are:

a) for an internal SATA cable the Maximum Rise Time shall be 85 ps measured from 20 % threshold to 80 % threshold; or

b) for an eSATA cable the Maximum Rise Time shall be 150 ps measured from 20 % threshold to 80 % threshold.

3.9.7 SI-06 : Intra-pair skew

3.9.7.1 Cable assembly expected behavior

See Section 6.12.2, Table 36 for internal and Table 37 for eSATA of the Serial ATA Revision 3.5.

3.9.7.2 Measurement requirements

The required measurements are:

a) this test is normative for internal SATA cables and informative for eSATA cables;
b) follow procedure P8 in Table 40 of Section 6.12.3.4 of the Serial ATA Revision 3.5; and
c) all cables and all adapters shall be de-skewed just prior to performing the measurement. Be aware that inclusion of the adapters in calibrations for other tests may not be correct.

3.9.7.3 Pass/fail criteria

The pass/fail requirements are:

a) for an internal SATA cable the Maximum Intra-Pair Skew shall not exceed 10 ps; or
b) for an eSATA cable the Maximum Intra-Pair Skew shall not exceed 20 ps.

3.9.8 SI-07 : Insertion loss

3.9.8.1 Cable assembly expected behavior

See Section 6.12.2, Table 36 for internal and Table 37 for eSATA of the Serial ATA Revision 3.5.

3.9.8.2 Measurement requirements

The required measurements are:

a) this test is normative for internal SATA cables and for eSATA cables;
b) follow procedure P5 in Table 40 of Section 6.12.3.4 of the Serial ATA Revision 3.5;
c) the test shall be performed in one direction on the cable assembly, for each differential pair of the assembly; and
d) if a family of cables is being tested, only the longest length is tested for this requirement.

3.9.8.3 Pass/fail criteria

The pass/fail requirements are:

a) for an internal SATA cable the Maximum Insertion Loss of the cable shall not exceed 6 dB (10 MHz to 4 500 MHz); or
b) for an eSATA cable the Maximum Insertion Loss of the cable shall not exceed 8 dB (10 MHz to 4 500 MHz).

3.9.9 SI-08 : Differential to differential crosstalk NEXT

3.9.9.1 Cable assembly expected behavior

See Section 6.12.2, Table 36 for internal and Table 37 for eSATA of the Serial ATA Revision 3.5.

3.9.9.2 Measurement requirements

The required measurements are:

a) this test is normative for internal SATA cables and for eSATA cables;
b) the test shall be performed on both ends of the cable assembly, but only needs to be measured in one direction on each end (e.g., with the Tx pair as the aggressor and the Rx pair as the receiver);
c) follow procedure P6 in Table 40 of Section 6.12.3.4 of the Serial ATA Revision 3.5;
d) if time-based test equipment is used to measure the near end crosstalk (NEXT), it shall use an acquisition window that is at least 4 times the propagation delay of the cable (electrical length); and
e) for test adapters comprising of 2 plugs to SMA and 1 receptacle to SMA adapters, each combination of plug / receptacle shall have a NEXT performance better than -36 dB (10 MHz to 4 500 MHz). The performance measurement of this adapter combination shall be

made and saved on a daily basis, or each time the setup is restored. In the event of a product failure, re-confirm that the adapter performance meets this requirement. For this measurement, the tester is required to continue to follow the same procedure for making a NEXT measurement on a product (see Procedure P6).

3.9.9.3 Pass/fail criteria

For an internal SATA or eSATA cable the Maximum Crosstalk shall not exceed NEXT -26 dB (10 MHz to 4 500 MHz).

3.9.10 SI-09 : Inter-symbol interference

3.9.10.1 Cable assembly expected behavior

See Section 6.12.2, Table 38 of the Serial ATA Revision 3.5.

3.9.10.2 Measurement requirements

The required measurements are:

a) this test is normative for internal SATA cables and for eSATA cables;
b) follow procedure P9 in Table 40 of Section 6.12.3.4 of the Serial ATA Revision 3.5;
c) the test shall be performed in one direction on the cable assembly, for each differential pair of the assembly;
d) if a family of cables is being tested, only the longest length is tested for this requirement;
e) as incident (test system induced) DJ shall not be de-convolved from the end results, it is critical to use a high quality (low jitter) fixture and stimulus system when performing this test; and
f) the 20 % to 80 % rise time and fall time of the pattern source shall be 136 ps, or as close to 136 ps as is practical, to minimize the resulting DJ and produce the most accurate results. Generate an LBP at 3.0 Gbps through the fixture.

3.9.10.3 Pass/fail criteria

For an internal SATA or eSATA cable the Maximum Inter-Symbol Interference shall not exceed 50 ps.

(Editor's Note: For legacy reasons, the mechanical sections of this document do not conform to the standard used in the rest of the document.)

3.10 Mechanical – device - standard internal connector

3.10.1 MDI-01 : Connector location

3.10.1.1 Device expected behavior

The device expected behavior is:

a) for a 12.7 mm Slimline optical device see Section 6.4.4.3.3, Figure 65 and Figure 67 of the Serial ATA Revision 3.5;
b) for a 9.5 mm Slimline optical device see Section 6.4.3.3, Figure 65 and Figure 66 of the Serial ATA Revision 3.5;
c) for a 7 mm Slimline optical device see Section 6.4.4.3.1, Figure 63 and Figure 68 of the Serial ATA Revision 3.5;
d) for a 5.25 inch optical device see Section 6.2.2, Figure 23 of the Serial ATA Revision 3.5;
e) for a 5.25 inch non-optical device see Section 6.2.2, Figure 24 of the Serial ATA Revision 3.5;
f) for a 3.5 inch side mounted device see Section 6.2.2, Figure 25 of the Serial ATA Revision 3.5;
g) for a 3.5 inch bottom mounted device see Section 6.2.2, Figure 26 of the Serial ATA Revision 3.5;
h) for a 2.5 inch side mounted device see Section 6.2.2, Figure 27 of the Serial ATA Revision 3.5;
i) for a 2.5 inch bottom mounted device see Section 6.2.2, Figure 28 of the Serial ATA Revision 3.5;
j) for a Micro SATA Connector for 1.8 inch HDD see Section 6.2.3, Figure 29 and Figure 30 of the Serial ATA Revision 3.5;
k) for a device mSATA Card see Section 6.6.3, Figure 94 and Figure 95 of the Serial ATA Revision 3.5; or
l) for a device M.2 Card (The details of the specification are found in the PCI Express M.2 Specification):

A) the mechanical parameters of this test are found in Section 6.9 of the Serial ATA Revision 3.5 as informative and the normative section of these parameters are contained in Section 2 of the PCI Express M.2 Specification; and
B) refer to the MOIs for additional test details and methodology.

3.10.1.2 Measurement requirements

Some measurements provide two or more reference planes (i.e., side mounting hole or bottom surface) depending on the implementation and are referenced with both a letter and number (i.e., a1 and a2). The required measurements are:

a) for a 12.7 mm Slimline optical device:
    a) from the bottom surface of the drive to the top of the tongue of the SATA plug shall be 6.20 mm ± 0.38mm;
    b) parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive shall be 0.40 mm;
    c) from the edge of the drive to the centerline of the SATA plug shall be 21.25 mm ± 0.38 mm; and
    d) from the back surface of the drive (i.e., the “end of the device factor”) to the base of the tongue of the SATA plug shall be 5.20 mm ± 0.3 mm;
b) for a 9.5 mm Slimline optical device:
    a) from the bottom surface of the drive to the top of the tongue of the SATA plug shall be 6.00 mm ± 0.38 mm;
    b) parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive shall be 0.40 mm;
    c) from the edge of the drive to the centerline of the SATA plug shall be 21.25 mm ± 0.38 mm; and
    d) from the back surface of the drive (i.e., the “end of the device factor”) to the base of the tongue of the SATA plug shall be 5.20 mm ± 0.3 mm;
c) for a 7 mm Slimline optical device:
    a) from the bottom surface of the drive to the top of the tongue of the SATA plug shall be 5.1 mm ± 0.38 mm;
    b) parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive shall be 0.40 mm;
    c) from the edge of the drive to the centerline of the SATA plug: shall be 21.25 mm ± 0.38 mm; and
    d) from the back surface of the drive (i.e., the “end of the device factor”) to the base of the tongue of the SATA plug shall be 5.20 mm ± 0.3 mm;
d) for a 5.25 inch optical device:
    a) from the bottom surface of the drive to the top of the tongue of the SATA plug shall be 10.00 mm ± 0.38 mm;
    b) parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive shall be 0.40 mm;
    c) from the centerline of the drive to the centerline of the SATA plug shall be 25.00 mm ± 0.38 mm; and
    d) from the back surface of the drive (i.e., the “end of the device factor”) to the base of the tongue of the SATA plug shall be 4.90 mm ± 0.50 mm;
e) for a 5.25 inch non-optical device:
    A) if the device follows Section 6.2.2, Figure 23, then use the pass/fail criteria for a *5.25 inch optical drive*; or
    B) if the device does not follow Section 6.2.2, Figure 23, then:
        a) from the bottom surface of the drive to the top of the tongue of the SATA plug shall be 3.50 mm ± 0.38 mm;
        b) parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive shall be 0.40 mm;
        c) from the centerline of the drive to the centerline of the SATA plug 42.90 mm ± 0.38 mm; and

d) from the back surface of the drive (i.e., the “end of the device factor”) to the base of the tongue of the SATA plug shall be 4.90 mm ± 0.50 mm;

f) for a 3.5 inch device:
   a1) from the centerline of the side mounting holes to the top of the tongue of the SATA plug shall be 2.85 mm ± 0.38 mm;
   a2) from the bottom surface of the drive to the top of the tongue of the SATA plug shall be 3.50 mm ± 0.38 mm;
   b) parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive shall be 0.25 mm;
   c) from the centerline of the drive to the centerline of the SATA plug shall be 20.68 mm ± 0.38 mm;
   d1) from the centerline of the side mounting holes to the base of the tongue of the SATA plug shall be 23.60 mm ± 0.50 mm;
   d2) from the centerline of the bottom mounting holes to the base of the tongue of the SATA plug 36.38 mm ± 0.50 mm;

g) for a 2.5 inch device:
   a1) from the centerline of the side mounting holes to the top of the tongue of the SATA plug shall be 0.50 mm ± 0.38 mm;
   a2) from the bottom surface of the drive to the top of the tongue of the SATA plug shall be 3.50 mm ± 0.38 mm;
   b) parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive shall be 0.25 mm;
   c) from the centerline of the drive to the centerline of the SATA plug shall be 4.80 mm ± 0.38 mm;
   d1) from the centerline of the side mounting holes to the base of the tongue of the SATA plug shall be 9.40 mm ± 0.50 mm; and
   d2) from the centerline of the bottom mounting holes to the base of the tongue of the SATA plug shall be 9.40 mm ± 0.50 mm.

h) for a Micro SATA Connector for 1.8 inch HDD:
   a) from the bottom surface of the drive to the top of the tongue shall be 78.5 mm ± 0.3 mm;
   b) parallelism of the top of the tongue of the SATA plug vs. the top surface of the drive shall be 0.40 mm maximum;
   c) from the centerline of the drive to the centerline of the SATA plug shall be 0.0 mm ± 0.20 mm;
   d) from the back surface of the drive (i.e., the “end of the device factor”) to the base of the tongue of the SATA plug shall be 4.9 mm ± 0.08 mm; and
   e) the Thickness of both sides of the drive shall be 3.30 mm ± 0.2 mm;

i) for a device mSATA Card:
   a) outer thickness of the board with components shall be a maximum of 4.85 mm;
   a1) top side thickness of soldered components shall be a maximum of 2.40 mm;
   a2) bottom side thickness of soldered components shall be a maximum of 1.35 mm;
   a3) bottom side clearance from connector base to first component shall be a minimum of 5.10 mm;
   a4) top side clearance from connector base to first component shall be a minimum of 3.20 mm;
   b) total length of the board shall be 50.80 mm ± 0.15 mm;
   b1) center hole to edge connector length shall be 48.05 mm ± 0.15 mm;
   b2) edge Finger connector length shall be 3.20 mm MIN;
   c) total width of the board shall be 29.85 mm ± 0.15 mm;
   c1) total width from center to center of assembly holes shall be 24.20 mm ± 0.15 mm;
   c2) short width from side to Edge Connector divider shall be 8.25 mm ± 0.15 mm;
   d) total width of board's Edge Connect shall be 25.70 mm ± 0.15 mm;
   d1) width of Edge Connector divider shall be 1.50 mm ± 0.10 mm;
   d2) width between center line of (pin 18 and pin 52) or (pin 17 and pin 51) shall be 13.60 mm ± 0.15 mm;
   d3) width between center line of (pin 1 and pin 15) or (pin 2 and pin 16) shall be 5.60 mm ± 0.15 mm; and

d4) width between center line of pins across edge connector divider (pin 15 and 17) or (pin 16 and 18) shall be 4.00 mm ± 0.15 mm;

or

j) for a device M.2 Card (The details of the specification are found in the PCI Express M.2 Specification):
    a) the mechanical parameters of this test are found in the Serial ATA Gold Specification Section 6.9 as informative and the normative section of these parameters are contained in Section 2 of the PCI Express M.2 Specification; and
    b) refer to the MOIs for additional test details and methodology.

3.10.1.3 Pass/fail criteria

All applicable measurements within this test shall pass for this test to pass.

3.10.2 MDI-02 : Visual and dimensional inspections

3.10.2.1 Device expected behavior

The expected device behavior is:

a) for Slimline optical device see Section 6.4.5.3.1, Figure 73, Figure 74, Figure 75, and Figure 76 of the Serial ATA Revision 3.5;
b) for Micro SATA HDDs see Section 6.3.5.1, Figure 59 of the Serial ATA Revision 3.5; or
c) for all other devices, see Section 6.2.10.3, Table 8, Section 6.2.2, Figure 29, and Section 6.2.3.1, Figure 32 and Figure 33 of the Serial ATA Revision 3.5.

3.10.2.2 Measurement requirements

The required measurements are:

a) for Slimline devices:
    a) the thickness of the device plug tongue shall be 1.23 mm ± 0.05 mm (Figure 76, section A-A);
    b) if the “Optional Wall” of Figure 76 is present, then the distance from the device plug tongue to the wall shall be 1.58 mm ± 0.08 mm (Figure 71, section A-A);
    c) if the “Optional Wall” of Figure 76 is not present, then there shall be a minimum of a 1.50 mm keep out zone from Datum A of Figure 75 to the nearest obstruction;
    d) the combined width of the power and signal segments shall be 20.4 mm ± 0.08 mm (Figure 75); and
    e) the separation between the power and signal segments shall be 2.34 mm ± 0.05 mm (Figure 75);
b) for Micro SATA devices:
    a) the thickness of the device plug tongue shall be 1.23 mm ± 0.05 mm (Figure 59, section C-C);
    b) the combined width of the power and signal segments shall be 27.04 mm ± 0.06 mm (Figure 59); and
    c) the separation between the power and signal segments shall be 2.41 mm ± 0.05 mm (Figure 59);

    or
c) for all other devices:
    a) the thickness of the device plug tongue shall be 1.23 mm ± 0.05 mm (Figure 33, section C-C);
    b) if the “Optional Wall” of Figure 33 is present, then the distance from the device plug tongue to the wall shall be 1.58 mm ± 0.08 mm (Figure 33, section B-B);
    c) if the “Optional Wall” of Figure 33 is not present, then there shall be a minimum of a 1.5 mm keep out zone from Datum A of Figure 33 to the nearest obstruction;
    d) the combined width of the power and signal segments shall be 33.39 mm ± 0.08 mm (Figure 32); and
    e) the separation between the power and signal segments shall be 2.41 mm ± 0.05 mm (Figure 32).

3.10.2.3 Pass/fail criteria

All applicable measurements within this test shall pass for this test to pass.

3.11 Mechanical – device - power connector

3.11.1 MDP-01 : Visual and dimensional inspections

3.11.1.1 Device expected behavior

The expected device behavior is:

a) for a Slimline optical device see Section 6.4.5.3.1, Figure 79 of the Serial ATA Revision 3.5;
b) for Micro SATA devices see Section 6.3.5.1, Figure 59 of the Serial ATA Revision 3.5; or
c) for all other devices, see Section 6.2.10.3, Table 8, Section 6.2.3.1, Figure 32, and Section 6.2.2, Figure 30 and Figure 31 of the Serial ATA Revision 3.5.

3.11.1.2 Measurement requirements

The required measurements are:

a) for Slimline devices:
    a) the thickness of the device plug tongue shall be 1.23 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 74, section A-A);
    b) if the “Optional Wall” of Figure 74 of Serial ATA Revision 3.5 is present, then the distance from the device plug tongue to the wall shall be 1.58mm ± 0.08 mm (see Serial ATA Revision 3.5 Figure 74, section A-A); and
    c) if the “Optional Wall” of Figure 74 of Serial ATA Revision 3.5 is not present, then there shall be a minimum of a 1.5 mm keep out zone from Datum A of Figure 74 of Serial ATA Revision 3.5 to the nearest obstruction;
b) for Micro SATA devices:
    a) the thickness of the device plug tongue shall be 1.23 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 59, section C-C);

    or
c) for all other devices:
    a) the thickness of the device plug tongue shall be 1.23 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 33, section C-C);
    b) if the “Optional Wall” of Figure 33 is present, then the distance from the device plug tongue to the wall shall be 1.58 mm ± 0.08 mm (see Serial ATA Revision 3.5 Figure 33, section B-B); and
    c) if the “Optional Wall” of Figure 33 of Serial ATA Revision 3.5 is not present, then there shall be a minimum of a 1.5 mm keep out zone from Datum A of Figure 33 in Serial ATA Revision 3.5 to the nearest obstruction.

3.11.1.3 Pass/fail criteria

All applicable measurements within this test shall pass for this test to pass.

3.12 Mechanical – host - standard internal connector

3.12.1 MHI-01 : Visual and dimensional inspections (informative)

3.12.1.1 Host Assembly Expected behavior

The expected device behavior is:

a) for a Slimline host, see Section 6.4.5.4, Figure 84 of the Serial ATA Revision 3.5; or
b) for all other hosts, see Section 6.2.5.1, Figure 37 of the Serial ATA Revision 3.5.

3.12.1.2 Measurement requirements

The required measurements are:

a) for Slimline hosts:
    a) inside width of Slimline Host Receptacle Connector shall be 20.6 mm ± 0.10 mm;
    b) width of key between power and signal segment shall be 2.04 mm ± 0.10 mm; and
    c) outside width of Slimline Host Receptacle Connector shall be 25.4 mm ± 0.15 mm;

    or
b) for all other hosts:

a) gap between tongue to edge of blind mate key shall be 1.65 mm ± 0.15 mm;
b) gap between tongue to blind mate key shall be 3.05 mm ± 0.08 mm;
c) gap between tongue and 2nd wall shall be a minimum of 1.10 mm;
d) width of tongue shall be 10.41 mm ± 0.08 mm;
e) width of short leg of "L" shall be 1.15 mm ± 0.05 mm;
f) depth of tongue (from tip to base) shall be 5.40 mm ± 0.08 mm;
g) inside width of the blind mate key shall be 2.20 mm ± 0.15 mm;
h) thickness of tongue shall be 1.23 mm ± 0.05 mm; and
i) gap between tongue and keep out or optional latching wall shall be 1.58 mm ± 0.08 mm.

3.12.1.3 Pass/fail criteria

All applicable measurements within this test shall pass for this test to pass.

3.13 Mechanical – drive/host – eSATA connector (informative)

3.13.1 MXE-01 : Visual and dimension inspection

3.13.1.1 Expected behavior

The expected device behavior is:
a) see Section 6.11.2.2, Figure 143 to Figure 148 of the Serial ATA Revision 3.5;
b) Figures 143 to Figure 148 of Serial ATA Revision 3.5 specify mechanical dimensions of the external RA SMT plug, RA SMT plug- reversed pin out, RA through-hole plug, vertical SMT plug, and vertical through-hole plug respectively; and
c) the following measurements use the RA SMT plug (Figure 105) as an example. Other types of plugs (see Serial ATA Revision 3.5 Figure 144 to Figure 148) shall follow the same criteria accordingly.

3.13.1.2 Measurement requirements

The required measurements are:
a) the height of the slot in RA SMT plug shall be 4.10 mm ± 0.1 mm (see Serial ATA Revision 3.5 Figure 144 to Figure 148);
b) the height of the slot (for receptacle key) shall be 1.50 mm ± 0.08 mm (see Serial ATA Revision 3.5 Figure 144 to Figure 148);
c) the thickness of the plug tongue shall be 1.20 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 144 to Figure 148);
d) the width of the plug tongue shall be 10.00 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 144 to Figure 148);
e) the width of the slot (for receptacle key) shall be 15.00 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 144 to Figure 148);
f) the width of the bottom slot (for receptacle wall) shall be 13.00 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 144 to Figure 148);
g) the width of the top slot (for receptacle) shall be 10.00 mm ± 0.05 mm (see Serial ATA Revision 3.5 Figure 144 to Figure 148);
h) the retention springs (x4) of the plug connector shall have the spring tip aligned with the datum (Y) within 4.10 mm ± 0.1 mm (see Serial ATA Revision 3.5 Figure 144 to Figure 148);
*i) informative - The retention springs (x4) of the plug connector shall have a width of 1.50 mm ± 0.1 mm (*see Serial ATA Revision 3.5 *Figure 144 to Figure 148);*
*j) informative - The retention springs (x4) of the plug connector shall be bilaterally located with the centerline within 6.80 mm ± 0.1 mm (*see Serial ATA Revision 3.5 *Figure 144 to Figure 148); and*
*k) informative - The length of the contact blades shall be 4.25 mm ± 0.1 mm for each of the 4 signal pins and 4.75 mm ± 0.1 mm for each of the 3 ground pins as measured from datum plane Y (*see Serial ATA Revision 3.5 *Figure 144 to Figure 148).*

3.13.1.3 Pass/fail criteria

All applicable measurements within this test shall pass for this test to pass.

3.14 Phy general requirements

3.14.1 PHY-01 : Unit interval

3.14.1.1 Device/host expected behavior

See Section 7.4.3.1.4 of Serial ATA Revision 3.5.

3.14.1.2 Measurement requirements

The required measurements are:

a) see section 7.6.16 of Serial ATA Revision 3.5;
b) for products which support 6 Gbps, this requirement shall be tested at all interface rates (1.5 Gbps, 3 Gbps, and 6 Gbps); and
c) in general, all interface rates claimed to be supported by the PUT shall be tested.

3.14.1.3 Pass/fail criteria

The pass/fail requirements are:

a) PHY-01a – the Mean Unit Interval shall measure between a minimum of 666.433 3 ps to a maximum of 670.233 3 ps for products running at 1.5 Gbps;
b) PHY-01b – the Mean Unit Interval shall measure between a minimum of 333.216 7 ps to a maximum of 335.116 7 ps for products running at 3 Gbps;
c) PHY-01c – the Mean Unit Interval measured between a minimum of 166.608 3 ps to a maximum of 167.558 3 ps for products running at 6 Gbps; and
d) the values above shall be based on at least 100 000 UIs (covers at least one SSC profile).

3.14.2 PHY-02 : Frequency long term accuracy

3.14.2.1 Device/host expected behavior

This test is not applicable to products that support SSC.

See Section 7.4.3.1.5 of Serial ATA Revision 3.5.

3.14.2.2 Measurement requirements

The required measurements are:

a) see Section 7.6.9 of Serial ATA Revision 3.5;
b) this test is only run once at the maximum interface rate of the product (1.5 Gbps, 3 Gbps, or 6 Gbps); and
c) the execution of this test shall include use of the frequency demodulator and low pass filter defined within Section 7.6.16 of Serial ATA Revision 3.5.

3.14.2.3 Pass/fail criteria

The f_{tol} shall be measured between -350 ppm and 350 ppm.

3.14.3 PHY-03 : Spread-spectrum modulation frequency

3.14.3.1 Device/host expected behavior

See Section 7.4.3.1.6 and Section 7.5.4 of Serial ATA Revision 3.5.

This test requires support for Spread Spectrum Clocking (SSC), which is optional.

3.14.3.2 Measurement requirements

The required measurements are:

a) see Section 7.6.16 of Serial ATA Revision 3.5; and
b) this test is only run once at the maximum interface rate of the product (1.5 Gbps, 3 Gbps, or 6 Gbps).

3.14.3.3 Pass/fail criteria

The pass/fail requirements are:

a) f_{SSC} measured between 30 kHz and 33 kHz; and
b) the value above shall be based on a mean of at least 10 complete SSC cycles.

3.14.4 PHY-04 : Spread-spectrum modulation deviation

3.14.4.1 Device/host expected behavior

See Section 7.4.3.1.7 and Section 7.5.4 of Serial ATA Revision 3.5.

This test requires support for Spread Spectrum Clocking (SSC), which is optional.

3.14.4.2 Measurement requirements

The required measurements are:
a) see Section 7.6.16 of Serial ATA Revision 3.5;
b) this test is only run once at the maximum interface rate of the product (1.5 Gbps, 3 Gbps, or 6 Gbps);
c) the value reported as the result shall be the single total range value relative to nominal of the SSC modulation deviation, using the equations below, where “Min” is the mean of 10 recorded values of the minimum peaks and “Max” is the mean of 10 recorded values of the maximum peaks;
d) calculate max deviation = (Measured Max – Nominal)/Nominal × 1e6 ppm; and
e) calculate min deviation = (Measured Min – Nominal)/Nominal × 1e6 ppm.

3.14.4.3 Pass/fail criteria

The pass/fail requirements are:
a) max SSC_{tol} shall be measured (using mean of 10 recorded values) less than +350 ppm; and
b) min SSC_{tol} shall be measured (using mean of 10 recorded values) greater than -5 350 ppm.

3.15 Phy transmitter requirements

3.15.1 Overview

During the testing execution for all Tx test requirements, it is essential that the product under test be able to complete an initial OOB sequence through the device COMWAKE. This is to allow product calibration to occur prior to and/or during the initial power on and detect sequences.

3.15.2 TX-01 : Pair differential impedance (informative)

3.15.2.1 Device/host expected behavior

See Section 7.4.3.2.2 of Serial ATA Revision 3.5.

3.15.2.2 Measurement requirements

The required measurements are:
a) see Section 7.6.28 of Serial ATA Revision 3.5;
b) this test requirement is only applicable to products running at 1.5 Gbps. For products which support 3 Gbps or 6 Gbps, this test is not required; and
c) testing of this requirement shall be completed during transmission of the Mid Frequency Test Pattern (MFTP). The amplitude of a TDR pulse or excitation applied to an active transmitter shall not exceed 139 mVpp (-13.2 dBm 50 ohm) single-ended.

3.15.2.3 Pass/fail criteria

Verify that both the minimum [TX-01a] and maximum [TX-01b] results for the pair differential impedance measured between 85 ohm and 115 ohm (for products running at 1.5 Gbps).

NOTE 388 - The verification of this result is conditional. If a 1.5 Gbps product passes TX-06, then it is not required that this test be verified but shall be verified for a 1.5 Gbps product if it fails TX-06.

3.15.3 TX-02 : Single-ended impedance (obsolete)

3.15.3.1 Device/host expected behavior

See Section 7.4.3.2.3 of Serial ATA Revision 3.5.

3.15.3.2 Measurement requirements

The required measurements are:

a) see Section 7.6.29 of Serial ATA Revision 3.5;
b) this test requirement is only applicable to products that support a maximum operating speed of 1.5 Gbps. For products that support a maximum operating speed of 3 Gbps or 6 Gbps this test is not required; and
c) testing of this requirement shall be completed during transmission of the MFTP. The amplitude of a TDR pulse or excitation applied to an active transmitter shall not exceed 139 mVpp (-13.2 dBm 50 ohm) single-ended.

3.15.3.3 Pass/fail criteria

The pass/fail requirements are:

a) $Z_{s\text{-}eTX}$ measured to be at least 40 ohm impedance; and
b) both the minimum [TX-02a] and the maximum [TX-02b] results shall be captured.

3.15.4 TX-03 : Gen2 (3 Gbps) differential mode return loss (informative)

3.15.4.1 Device/host expected behavior

See Section 7.4.3.2.4 of Serial ATA Revision 3.5.

3.15.4.2 Measurement requirements

The required measurements are:

a) see Section 7.4.3.2.4 of Serial ATA Revision 3.5;
b) calibrate to the end of the SMA cables but do *not* include (de-embed) the SMA to SATA PCB and the SATA connector so the board and the SATA connector are *included* with the product measurement;
c) this test requirement is only applicable to products that support a maximum operating speed of 3 Gbps. For products that support a maximum operating speed of 6 Gbps this test is not required; and
d) testing of this requirement shall be completed during transmission of the MFTP. The amplitude of a TDR pulse or excitation applied to an active transmitter shall not exceed 139 mVpp (-13.2 dBm 50 ohm) single-ended.

3.15.4.3 Pass/fail criteria

The $RL_{DD11,TX}$ is measured per the values in Section 7.4.2, Table 53 (for products running at 3 Gbps):

Table 2 - TX Differential Mode Return Loss for 3 Gbps

Test name	Frequency	Minimum (dB)
TX-03a	150 MHz to 300 MHz	14
TX-03b	300 MHz to 600 MHz	8
TX-03c	600 MHz to 1.2 GHz	6
TX-03d	1.2 GHz to 2.4 GHz	6
TX-03e	2.4 GHz to 3.0 GHz	3
TX-03f	3.0 GHz to 5.0 GHz	1 (na for Gen2m)

3.15.5 TX-04 : Gen2 (3 Gbps) common mode return loss (informative)

3.15.5.1 Device/host expected behavior

See Section 7.4.3.2.5 of Serial ATA Revision 3.5.

3.15.5.2 Measurement requirements

The required measurements are:

a) see Section 7.6.15 of Serial ATA Revision 3.5;
b) calibrate to the end of the SMA cables but do *not* include (de-embed) the SMA to SATA PCB and the SATA connector so the board and the SATA connector are *included* with the product measurement;
c) this test requirement is only applicable to products that support a maximum operating speed of 3 Gbps. For products that support a maximum operating speed of 1.5 Gbps or 6.0 Gbps this test is not required; and
d) testing of this requirement shall be completed during transmission of the MFTP. The amplitude of a TDR pulse or excitation applied to an active transmitter shall not exceed 139 mVpp (-13.2 dBm 50 ohm) single-ended.

3.15.5.3 Pass/fail criteria

The $RL_{CC11,TX}$ is measured per the values in Section 7.4.3.2.5 of Serial ATA Revision 3.5 for products running at 3 Gbps.

Table 3 - TX Common Mode Return Loss for 3 Gbps

Test name	Frequency	Minimum (dB)
TX-04a	150 MHz to 300 MHz	8 Gen2i, 5 Gen2m
TX-04b	300 MHz to 600 MHz	5
TX-04c	600 MHz to 1.2 GHz	2
TX-04d	1.2 GHz to 2.4 GHz	1
TX-04e	2.4 GHz to 3.0 GHz	1
TX-04f	3.0 GHz to 5.0 GHz	1 (na for Gen2m)

3.15.6 TX-05 : Gen2 (3 Gbps) impedance balance (informative)

3.15.6.1 Device/host expected behavior

See Section 7.4.3.2.6 of Serial ATA Revision 3.5.

3.15.6.2 Measurement requirements

The required measurements are:

a) see Section 7.6.15 of Serial ATA Revision 3.5;
b) for products that support a maximum operating speed of 1.5 Gbps this test is not required;
c) impedance balance is defined as the ratio (expressed in dB) of common mode incident power at a 25 ohm impedance level to differential mode reflected power at a 100 ohm impedance level. The impedance balance is a bound on the coupling between common and differential modes; and
d) testing of this requirement shall be completed during transmission of the MFTP. The amplitude of a TDR pulse or excitation applied to an active transmitter shall not exceed 139 mVpp (-13.2 dBm 50 ohm) single-ended.

3.15.6.3 Pass/fail criteria

The $RL_{DC11,TX}$ is measured per the values in Section 7.4.3.2.6 of Serial ATA Revision 3.5 (for products running at 3 Gbps).

Table 4 - TX Impedance Balance

Test Name	Frequency	Minimum (dB)
TX-05a	150 MHz to 300 MHz	30
TX-05b	300 MHz to 600 MHz	20
TX-05c	600 MHz to 1.2 GHz	10
TX-05d	1.2 GHz to 2.4 GHz	10
TX-05e	2.4 GHz to 3.0 GHz	4
TX-05f	3.0 GHz to 5.0 GHz	4 (na for Gen2m)

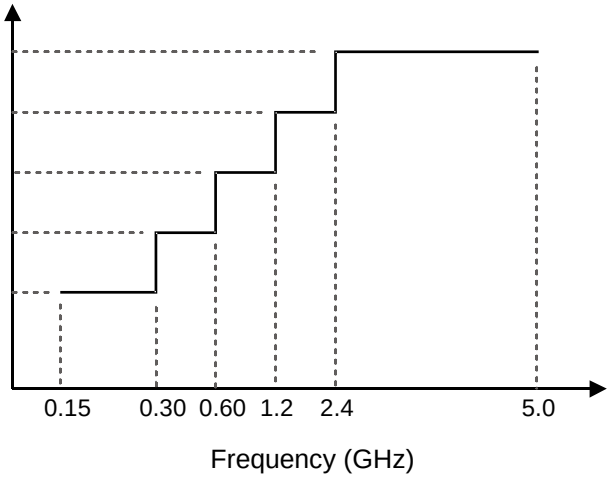


Figure 177 from Serial ATA Revision 3.5 Section 7.4.3.2.6

3.15.7 TX-06 : Gen1 (1.5 Gbps) Differential mode return loss (Informative)

3.15.7.1 Device/host expected behavior

See Section 7.4.3.2.7 of Serial ATA Revision 3.5.

3.15.7.2 Measurement requirements

The required measurements are:

a) see Section 7.6.15 of Serial ATA Revision 3.5;
b) calibrate to the end of the SMA cables but do *not* include (de-embed) the SMA to SATA PCB and the SATA connector so the board and the SATA connector are *included* with the product measurement;
c) this test requirement is only applicable to products running at 1.5 Gbps. For products which support 3 Gbps, this test is not required; and
d) testing of this requirement shall be completed during transmission of the MFTP. The amplitude of a TDR pulse or excitation applied to an active transmitter shall not exceed 139 mVpp (-13.2 dBm 50 ohm) single-ended.

3.15.7.3 Pass/fail criteria

The $RL_{DD11,TX}$ is measured per the values in Table 5 (for products running at 1.5 Gbps).

Table 5 - TX Differential Mode Return Loss for 1.5 Gbps

Test name	Frequency	Minimum (dB)
TX-06a	75 MHz to 150 MHz	14
TX-06b	150 MHz to 300 MHz	8
TX-06c	300 MHz to 600 MHz	6
TX-06d	600 MHz to 1.2 GHz	6
TX-06e	1.2 GHz to 2.4 GHz	3
TX-06f	2.4 GHz to 3.0 GHz	1 (na for Gen1m)

3.15.8 TX-07 : Gen3 (6 Gbps) differential mode return loss (informative)

3.15.8.1 Device/host expected behavior

See Section 7.4.3.2.7 and Section 7.6.15 of Serial ATA Revision 3.5.

3.15.8.2 Measurement requirements

The required measurements are:

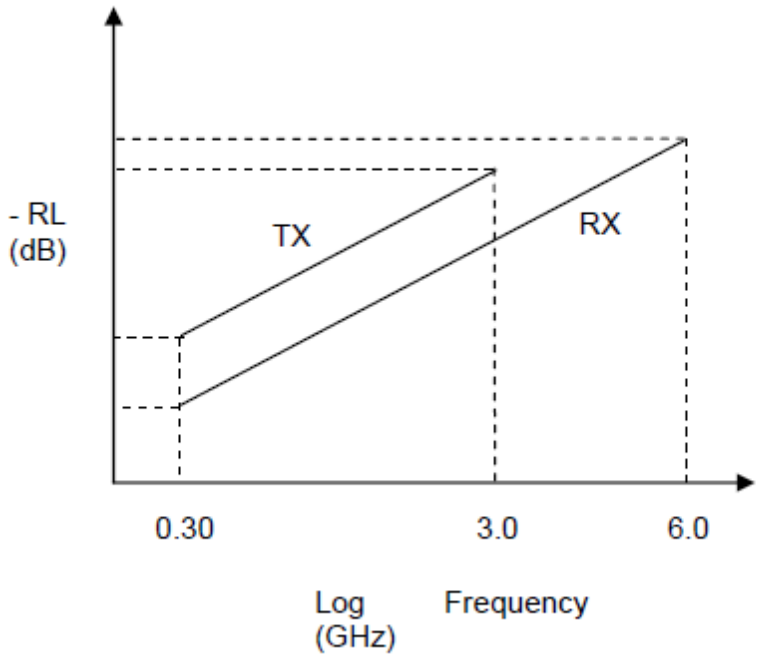
a) calibrate to the end of the SMA cables but do *not* include (de-embed) the SMA to SATA PCB and the SATA connector so the board and the SATA connector are *included* with the product measurement;
b) this test requirement is only applicable to products that support a maximum operating speed of 6 Gbps. For products that support a maximum operating speed of 1.5 Gbps or 3 Gbps, this test is not required; and
c) testing of this requirement shall be completed during transmission of the MFTP. The amplitude of a TDR pulse or excitation applied to an active transmitter shall not exceed 139 mVpp (-13.2 dBm 50 ohm) single-ended.

3.15.8.3 Pass/fail criteria

The $RL_{DD11,TX}$ is measured per the values in Section 7.4.2 Table 53 of Serial ATA Revision 3.5 (for products running at 6 Gbps).

NOTE 49 - The Return loss limit line starts at 300 MHz at -14 dB increasing at 13 dB/decade to 3 GHz.

Figure 2 - Tx Differential Mode Return Loss for 6 Gbps Figure



3.15.9 TX-08 : Gen3 (6 Gbps) impedance balance (informative)

3.15.9.1 Device/host expected behavior

See Section 7.4.3.2.6 of Serial ATA Revision 3.5.

3.15.9.2 Measurement requirements

The required measurements are:

a) see Section 7.6.15 of Serial ATA Revision 3.5;
b) this test requirement is only applicable to products that support a maximum operating speed of 6 Gbps. For products that support a maximum operating speed of 1.5 Gbps or 3 Gbps, this test is not required;
c) impedance balance is defined as the ratio (expressed in dB) of common mode incident power at a 25 ohm impedance level to differential mode reflected power at a 100 ohm impedance level. The impedance balance is a bound on the coupling between common and differential modes; and
d) testing of this requirement shall be completed during transmission of the MFTP. The amplitude of a TDR pulse or excitation applied to an active transmitter shall not exceed 139 mVpp (-13.2 dBm 50 0ohm) single ended.

3.15.9.3 Pass/fail criteria

The $RL_{DC11,TX}$ is measured per the values:

Table 6 - TX Impedance Balance

Test Name	Frequency	Minimum (dB)
TX-08a	150 MHz to 300 MHz	30
TX-08b	300 MHz to 600 MHz	30
TX-08c	600 MHz to 1.2 GHz	20
TX-08d	1.2 GHz to 2.4 GHz	10
TX-08e	2.4 GHz to 3 GHz	10
TX-08f	3 GHz to 5 GHz	4
TX-08g	5 GHz to 6.5 GHz	4

Table 53 of Serial ATA Revision 3.5

3.16 Phy transmit signal requirements

3.16.1 Overview

During the testing execution for all TSG test requirements, it is essential that the product under test be able to complete an initial OOB sequence through the device COMWAKE prior to transmission of a BIST FIS or initiation of the BIST mode sequence. This is to allow product calibration to occur prior to and/or during the initial power on and detect sequences.

Tester is required to save all the calibration data (i.e., screen shot) that is done daily at a minimum, if not every device evaluation. Valid calibration data shall be available per product for review, even if the same calibration data (i.e., daily) is used for multiple products. It is required that calibration be completed for this area of testing to ensure consistent measurements and environment impacts.

3.16.2 TSG-01 : Differential output voltage

3.16.2.1 Device/host expected behavior

See Section 7.4.3.3.2 of Serial ATA Revision 3.5.

3.16.2.2 Measurement requirements

The required measurements are:

a) see Section 7.6.5 of Serial ATA Revision 3.5;
b) for products which support 3 Gbps, this requirement shall be tested at both interface rates (1.5 Gbps and 3 Gbps);
c) for the interests of the Interoperability Program, the measurements shall only be taken to verify this requirement at the minimum limit. Within the Specification, there are two options for measuring the minimum:
    A) Vtest = min(DH, DM, VtestLBP) – 1.5 Gbps [TSG-01a], 3 Gbps [TSG-01g]; or
    B) Vtest = min(DH, DM, VtestAPP) – 1.5 Gbps [TSG-01b], 3 Gbps [TSG-01h];
d) gathering a minimum result from either of the options above is acceptable. It is not required to report a result for both; and
e) the pu/pl measurements outlined in the Specification shall be taken but the results are informative. Verification of maximum limit values for this measurement is not required.

Pattern	Interface Rate	
	1.5 Gbps	3 Gbps
MFTP – pu	TSG-01c	TSG-01i
MFTP – pl	TSG-01d	TSG-01j
LFTP – pu	TSG-01e	TSG-01k
LFTP – pl	TSG-01f	TSG-01l

Table 7 – Diff Output Voltage pu/pl Test Name Matrix

3.16.2.3 Pass/fail criteria

The minimum V_{diffTX} is measured for products running at 1.5 Gbps and 3 Gbps shall be at least 400 mVppd.

3.16.3 TSG-02 : Rise/fall time (informative)

3.16.3.1 Device/host expected behavior

See Section 7.4.3.3.4 of Serial ATA Revision 3.5.

3.16.3.2 Measurement requirements

The required measurements are:

a) see Section 7.6.6 of Serial ATA Revision 3.5;
b) for products which support 3 Gbps, this requirement shall be tested at each of the 1.5 Gbps and 3 Gbps interface rates;
c) for products which support 6 Gbps, this requirement shall be tested at each of the 1.5 Gbps, 3 Gbps, and 6 Gbps interface rates;
d) the LFTP pattern defined in Section 4.1.1.87 of the Serial ATA Revision 3.5 is used for all Rise time and Fall time measurements to ensure consistency;
e) the Rise and Fall times of the waveform under test are defined over a 20 % to 80 % output level change from the High and Low reference levels. The High reference level of the waveform under test is the “mode” of the top portion while the Low reference level is the “mode” of the bottom portion. Mode is measured using Statistical Methods of the desired waveform and is the most common value of the probability density function. The minimum time span of the analysis zone for measuring the mode amplitude shall be 8 UI;
f) Rise Time = X2 - X1, where X2 is the mean horizontal time value corresponding to 80 % of the distance between the Low and High value and X1 is the mean horizontal time value position corresponding to 20 % of the distance between the Low and High value;
g) Fall Time = X1 - X2, where X1 is the mean horizontal time value corresponding to 20 % of the distance between the Low and High value and X2 is the mean horizontal time value position corresponding to 80 % of the distance between the Low and High value;
h) for Gen3i, the Rise and Fall time values, between 20 % and 80 %, are measured using only the Gen3 LFTP. This minimizes errors in determining the 0 % and 100 % reference levels using the Mode Amplitude measurement method. The analysis zone of the measurement shall be made over a minimum time length of 8 UI. This is a Lab Load measurement. The Rise and Fall time compliance limits, for the differential Tx test pattern are listed in Table 31. The average Rise time of all rising edges and the separate average Fall time of all falling edges within the analysis zone shall meet the Rise and Fall time compliance limits respectively; and
i) in order to ensure efficient test time of products within the Interoperability Testing, testing of this requirement shall be limited to the LFTP as defined in the Serial ATA Revision 3.5. The HFTP pattern measurements have been obsolete with the introduction of Unified Test Document 1.4, per a ratified change to Serial ATA Revision 3.1.

Pattern	Interface Rate		
	1.5 Gbps	3 Gbps	6 Gbps
HFTP rise (obsolete)	TSG-02a (obsolete)	TSG-02c (obsolete)	n/a
HFTP fall (obsolete)	TSG-02b (obsolete)	TSG-02d (obsolete)	n/a
LFTP rise	TSG-02e	TSG-02f	TSG-02i
LFTP fall	TSG-02g	TSG-02h	TSG-02j

Table 8 – Tx Rise/Fall Test Name matrix

3.16.3.3 Pass/fail criteria

The $t_{20\text{-}80TX}$ is measured per the Max values in Table 9 for LFTP pattern.

NOTE 50 - Failures at minimum rate have not been shown to affect interoperability and shall not be included in determining pass/fail.

Limit	Time @ 1.5 Gbps (ps (UI))	Time @ 3 Gbps (ps (UI))	Time @ 6 Gbps (ps (UI))
Min 20 % to 80 %	50 (0.075)	50 (0.15)	33 (0.20)
Max 20 % to 80 %	273 (0.41)	136 (0.41)	80 (0.48)

Table 9 - Tx Rise/Fall Time

3.16.4 TSG-03 : Differential skew (informative)

3.16.4.1 Device/host expected behavior

See Section 7.4.3.3.5 of Serial ATA Revision 3.5.

3.16.4.2 Measurement requirements

The required measurements are:

a) see Section 7.4.17 of Serial ATA Revision 3.5;
b) this test is only run once at the maximum interface rate of the product, either 1.5 Gbps, 3 Gbps, or 6 Gbps;
c) DC blocks or software/hardware equivalent shall be used; and
d) this test requires measuring the mean skew of Tx+ rise mid-point to the Tx- fall mid-point and the mean skew of Tx+ fall mid-point to Tx- rise mid-point, as stated in Section 7.4.3.3.5, and then computing the Differential Skew = average of the magnitude (absolute value) of the two mean skews. This removes the effect of rise-fall imbalance from the skew measurement.

3.16.4.3 Pass/fail criteria

The t_{skewTX} is measured at a maximum of 20 ps based on at least 10 000 UIs.

3.16.5 TSG-04 : AC common mode voltage

3.16.5.1 Device/host expected behavior

See Section 7.4.3.3.6 of Serial ATA Revision 3.5.

3.16.5.2 Measurement requirements

The required measurements are:

a) see Section 7.4.3.3.6 and Section 7.6.22 of Serial ATA Revision 3.5;
b) the required test pattern is D24.3 (MFTP) for Gen1u, Gen2u, Gen2i Gen2m, Gen3i, and Gen3u;
c) the required test pattern is D10.2 (HFTP) for Gen1u, Gen2u, Gen3i, and Gen3u;
d) the analysis bandwidth shall be limited on the low end at 200 MHz (see Serial ATA Revision 3.5 Section 7.6.22) and the High by specified requirements of Fbaud/2 (Fundamental) with a 1st order filter roll off response; and
e) see Table 55 (General Electrical) of Serial ATA Revision 3.5 for Gen1u, Gen2u, and Gen3u UHost based on electrical specifications.

3.16.5.3 Pass/fail criteria

The pass/fail requirements are:

a) $V_{cm,acTX}$ measured at a maximum of:
   A) 50 mVpp for Gen2i and Gen2m;
   B) 100 mVpp for Gen1u and Gen2u; or
   C) 120 mVpp for Gen3i and Gen3u;
   and
b) based on at least 10 000 UIs.

3.16.6 TSG-05 : Rise/fall Imbalance (obsolete)

3.16.6.1 Device/host expected behavior

See Section 7.4.3.3.11 of Serial ATA Revision 3.5.

3.16.6.2 Measurement requirements

The required measurements are:

a) see Section 7.6.21 of Serial ATA Revision 3.5;
b) this test requirement is only applicable to products running at 3 Gbps; and
c) reference TSG-02 for details as these may apply to TSG-05.

From Edge	To Edge	Test Name		
		HFTP	MFTP	LFTP
Tx+ rise	Tx- fall	TSG-05a (obsolete)	TSG-05c (obsolete)	TSG-05e (obsolete)
Tx+ fall	Tx- rise	TSG-05b (obsolete)	TSG-05d (obsolete)	TSG-05f (obsolete)

Table 10 – Rise / Fall Imbalance test name matrix

3.16.6.3 Pass/fail criteria

For products running at 3 Gbps, Mean R/F_{bal} measured at a maximum of 20 % based on at least 10 000 UIs.

3.16.7 TSG-06 : Amplitude imbalance (obsolete)

3.16.7.1 Device/host expected behavior

See Section 7.4.3.3.12 of Serial ATA Revision 3.5.

3.16.7.2 Measurement requirements

The required measurements are:

a) see Section 7.4.3.3.12 of Serial ATA Revision 3.5;
b) this test requirement is only applicable to products running at 3 Gbps;
c) due to characteristics of the MFTP, it is required the measurement points be taken at 0.5 UI of the second bit within the pattern. All amplitude values for this measurement shall be the statistical mode measured at 0.5 UI nominal over a minimum of 10 000 UI;
d) the amplitude imbalance (Amp_{bal}) for each UI shall be computed using the following formula (directly from Section 7.4.3.3.12 of Serial ATA Revision 3.5), ABS(Tx+ amplitude – Tx- amplitude) / ((Tx+ amplitude + Tx- amplitude)/2); and
e) results for HFTP [TSG-06a] and MFTP [TSG-06b] shall be captured.

3.16.7.3 Pass/fail criteria

The Amp_{bal} shall not exceed a maximum of 10 % (for products running at 3 Gbps).

3.16.8 TSG-07 : Gen1 (1.5 Gbps) TJ at connector, clock to data, $f_{BAUD}/10$ (obsolete)

These measurements are no longer defined in Serial ATA Revision 3.2 or later.

3.16.9 TSG-08 : Gen1 (1.5 Gbps) DJ at connector, clock to data, $f_{BAUD}/10$ (obsolete)

These measurements are no longer defined in Serial ATA Revision 3.2 or later.

3.16.10 TSG-09 : Gen1 (1.5 Gbps) TJ at connector, clock to cata, $f_{BAUD}/500$

3.16.10.1 Device/host expected behavior

See Section 7.4.3.3.13 and Section 7.5 of Serial ATA Revision 3.5.

3.16.10.2 Measurement requirements

The required measurements are:

a) see Section 7.6.10 and Section 7.6.11 of Serial ATA Revision 3.5;
b) for products which support 3 Gbps or 6 Gbps, this requirement shall also be tested at 1.5 Gbps;
c) the Jitter Transfer Function (JTF) for the Jitter Measurement Device (JMD) is required to be per Section 7.5.3.1 and Section 7.5.3.2 of Serial ATA Revision 3.5;
d) additionally see Table 55 (General Electrical) of Serial ATA Revision 3.5 for Gen1u, Gen2u, and Gen3u UHost based on electrical specifications;
e) there are several different patterns defined within the Specification and are intended to be used to verify this requirement. In order to ensure efficient test time of products within the Interoperability Testing, testing of this requirement shall be limited to the following patterns as defined in the Serial ATA Revision 3.5 using High Frequency Test Pattern (HFTP) [TSG-09a] and LBP [TSG-09b]. It is optional to additionally test using the Simultaneous Switching Outputs Pattern (SSOP) [TSG-09c] as a third pattern; and
f) for this test, the methodology of obtaining the result shall follow the Clock-to-Data Transmit Jitter method outlined in Section 7.4.3.3.13 of Serial ATA Revision 3.5, similar to that for obtaining 3 Gbps results for TSG-11 and TSG-12. In the past, a Data-to-Data Transmit Jitter (see Appendix E.2 in Serial ATA Revision 3.5) method was used but is no longer preferred for the use of the interoperability testing.

3.16.10.3 Pass/fail criteria

The TJ is measured to a maximum limit of 0.37 UI when measured using the specified JTF for products running at 1.5 Gbps.

NOTE 51 - Due to the nature of taking this measurement with the Clock-to-Data method, the Specification requirement is aligned to that of the Clock-to-Data requirement of 3 Gbps products.

3.16.11 TSG-10 : Gen1 (1.5 Gbps) DJ at connector, clock to data, $f_{BAUD}/500$

3.16.11.1 Device/host expected behavior

See Section 7.4.3.3.13 and Section 7.5 of Serial ATA Revision 3.5.

3.16.11.2 Measurement requirements

The required measurements are:

a) see Section 7.6.10 and Section 7.6.11 of Serial ATA Revision 3.5;
b) for products which support 3 Gbps or 6 Gbps, this requirement shall also be tested at 1.5 Gbps;
c) the JTF for the Jitter JMD is required to be per Section 7.5.3.2 and Section 7.5.3.3 of Serial ATA Revision 3.5;
d) additionally see Table 55 (General Electrical) of Serial ATA Revision 3.5 for Gen1u, Gen2u, Gen3u UHost based on electrical specifications;
e) there are several different patterns defined within the Specification and are intended to be used to verify this requirement. In order to ensure efficient test time of products within the Interoperability

Testing, testing of this requirement shall be limited to the following patterns as defined in the Serial ATA Revision 3.5 using High Frequency Test Pattern (HFTP) [TSG-10a] and Lone Bit Pattern (LBP) [TSG-10b]. It is optional to additionally test using the SSOP [TSG-10c] as a third pattern; and

f) for this test, the methodology of obtaining the result shall follow the Clock-to-Data Transmit Jitter method outlined in Section 7.4.3.3.13 in Serial ATA Revision 3.5, similar to that for obtaining 3 Gbps results for TSG-11 and TSG-12. In the past, a Data-to-Data Transmit Jitter (see Appendix E.2 in Serial ATA Revision 3.5) method was used but is no longer preferred for the use of the interoperability testing.

3.16.11.3 Pass/fail criteria

The DJ is measured to a maximum limit of 0.19 UI when measured using the specified JTF for products running at 1.5 Gbps.

NOTE 52 - Due to the nature of taking this measurement with the Clock-to-Data method, the Specification requirement is aligned to that of the Clock-to-Data requirement of 3 Gbps products.

3.16.12 TSG-11 : Gen2 (3 Gbps) TJ at connector, clock to data, $f_{BAUD}/500$

3.16.12.1 Device/host expected behavior

See Section 7.4.3.3.13 and Section 7.5 of Serial ATA Revision 3.5.

3.16.12.2 Measurement requirements

The required measurements are:

a) see Section 7.6.10 and Section 7.6.11 of Serial ATA Revision 3.5;
b) this test requirement is only applicable to products running at 3 Gbps;
c) the JTF for the JMD is required to be calibrated per Section 7.5.3.2 and Section 7.5.3.3 of Serial ATA Revision 3.5;
d) additionally see Table 55 (General Electrical) of Serial ATA Revision 3.5 for Gen1u, Gen2u, Gen3u UHost based on electrical specifications; and
e) there are several different patterns defined within the Specification and are intended to be used to verify this requirement. In order to ensure efficient test time of products within the Interoperability Testing, testing of this requirement shall be limited to the following patterns as defined in the Serial ATA Revision 3.5 using High Frequency Test Pattern (HFTP) [TSG-11a] and LBP [TSG-11b]. It is optional to additionally test using the SSOP [TSG-11c] as a third pattern.

3.16.12.3 Pass/fail criteria

The TJ is measured to a maximum limit of 0.37 UI when measured using the specified JTF for products running at 3 Gbps.

3.16.13 TSG-12 : Gen2 (3 Gbps) DJ at connector, clock to data, $f_{BAUD}/500$

3.16.13.1 Device/host expected behavior

See Section 7.4.3.3.13 and Section 7.5 of Serial ATA Revision 3.5.

3.16.13.2 Measurement requirements

The required measurements are:

a) see Section 7.6.10 and Section 7.6.11 of Serial ATA Revision 3.5;
b) this test requirement is only applicable to products running at 3 Gbps;
c) the JTF for the JMD is required to be per Section 7.5.3.2 and Section 7.5.3.3 of Serial ATA Revision 3.5;
d) additionally, see Table 55 (General Electrical) of Serial ATA Revision 3.5 for Gen1u, Gen2u, Gen3u UHost based on electrical specifications; and
e) there are several different patterns defined within the Specification and are intended to be used to verify this requirement. In order to ensure efficient test time of products within the Interoperability Testing, testing of this requirement shall be limited to the following patterns as defined in the

Serial ATA Revision 3.5, High Frequency Test Pattern (HFTP) [TSG-12a] and Lone Bit Pattern (LBP) [TSG-12b]. It is optional to additionally test using the SSOP [TSG-12c] as a third pattern.

3.16.13.3 Pass/fail criteria

The DJ is measured to a maximum limit of 0.19 UI when measured using the specified JTF (for products running at 3 Gbps).

3.16.14 TSG-13: Gen3 (6 Gbps) transmit jitter

3.16.14.1 Device/host expected behavior

See Section 7.4.3.3.13 and Section 7.5 of Serial ATA Revision 3.5.

3.16.14.2 Measurement requirements

The required measurements are:

a) see Section 7.6.10 and Section 7.6.12 of Serial ATA Revision 3.5;
b) this test requirement is only applicable to products running at 6 Gbps;
c) the JTF for the JMD is required to be per Section 7.5.3.4 of Serial ATA Revision 3.5;
d) the Compliance Interconnect Channel (CIC) for the TJ measurements is required for Gen3i PUTs per Section 7.4.8 of Serial ATA Revision 3.5;
e) for a Gen3u UHost PUT, the Gen3i CIC channel is not used and the measurement is made directly into the lab load. Additionally see Table 55 (General Electrical) of Serial ATA Revision 3.5 for Gen1u, Gen2u, Gen3u UHost based on electrical specifications;
f) the methods used for Gen3i Transmit Jitter testing are intended to minimize RJ measurement error and allow for the TJ to be verified by a full population BERT scan as described in Section 7.6.10. This method also puts an upper limit on both DJ and RJ so neither may dominate the TJ;
g) the Transmit Jitter values specified in Table 54 of Serial ATA Revision 3.5, refer to the output signal from the unit under test (UUT) at the mated connector into a Laboratory Load (LL) from the unit under test through a CIC into a Laboratory Load when measuring TJ. All the interconnect characteristics of the transmitter, package, printed circuit board traces, and mated connector pair are included in the measured transmitter jitter. Since the SATA adapter is also included as part of the measurement, good matching and low loss in the adapter are desirable to minimize its contributions to the measured transmitter jitter; and
h) the TJ is measured with LBP. Measurements with all other patterns (HFTP, MFTP, and LFTP) are informative.

3.16.14.3 Pass/fail criteria

The pass/fail requirements are:

a) TJ (BER of 1E-12) measured at a maximum of 0.52 UI into a Laboratory Load after the CIC (for Gen3i PUT) or without the CIC (for Gen3u UHost PUT) using the specified JTF (for products running at 6 Gbps); and
b) TJ (BER of 1E-6) measured at a maximum of 0.46 UI into a Laboratory Load after the CIC (for Gen3i PUT) or without the CIC (for Gen3u UHost PUT) using the specified JTF (for products running at 6 Gbps).

3.16.15 TSG-14 : Gen3 (6 Gbps) Tx maximum differential voltage amplitude

3.16.15.1 Device/host expected behavior

See Section 7.4.3.3.2 of Serial ATA Revision 3.5.

3.16.15.2 Measurement requirements

The required measurements are:

a) see Section 7.6.4.3 and Section 7.6.7.3 of Serial ATA Revision 3.5 for a detailed description of this requirement;
b) this test requirement is only applicable to products running at the 6 Gbps interface rate;
c) testing of this requirement is limited to the differential of the MFTP as defined in the Serial ATA Revision 3.5;

d) the maximum differential amplitude shall be measured at the Tx Compliance point into a Lab Load. The connection required for this test is shown in Figure 217 of Serial ATA Revision 3.5;
e) the maximum amplitude is defined as the peak to peak value of the average of 500 waveforms measured over a time span of 4 Gen3 UI, using the HBWS; and
f) for this test, the differential MFTP signal is captured in a time span for each waveform encompassing 4 Gen3 unit intervals (4 × 166.6 ps). The Peak-to-Peak Amplitude over a 4 UI epoch, for a minimum of 500 acquisitions (2 000 UI) time averaged waveforms, is compared to the Pass/fail criteria. See Table 54 of Serial ATA Revision 3.5.

3.16.15.3 Pass/fail criteria

The differential voltage [(Tx+) – (Tx-)] measured shall be a maximum of 900 mVppd.

3.16.16 TSG-15 : Gen3 (6 Gbps) Tx minimum differential voltage amplitude

3.16.16.1 Device/host expected behavior

See Section 7.4.3.3.2 of Serial ATA Revision 3.5.

3.16.16.2 Measurement requirements

The required measurements are:
a) see Section 7.6.5 of Serial ATA Revision 3.5 for a detailed description of this requirement;
b) this test requirement is only applicable to products running at the 6 Gbps interface rate;
c) testing of this requirement is limited to the differential of the Gen3 LBP as defined in Section 7.4.5.4.6 of Serial ATA Revision 3.5;
d) the minimum Tx differential amplitude is a measurement of the minimum eye opening, using the specified method, after the Gen3i CIC, terminated into a Lab Load as specified in Section 7.4.8 of Serial ATA Revision 3.5. The connection required for this test is shown in Figure 216 and Figure 217 of Serial ATA Revision 3.5;
e) for a Gen3u UHost PUT, the Gen3i CIC channel is not used and the measurement is made directly into the lab load;
f) data is captured using the Gen3i Reference Clock JTF defined in Section 7.5.3.3 of Serial ATA Revision 3.5; and
g) for this test the amplitude distribution shall be measured to include a minimum of 5×10^6 Unit Intervals of data the eye height at the 50 % location of the bit interval shall be evaluated and compared to the Pass/fail criteria.

3.16.16.3 Pass/fail criteria

The differential voltage [(Tx+) – (Tx-)] measured shall be a minimum of 240 mVppd for a device and a minimum of 200 mVppd for a host.

3.16.17 TSG-16 : Gen3 (6 Gbps) Tx AC common mode voltage (obsolete)

3.16.17.1 Device/host expected behavior

See Section 7.6.23 of Serial ATA Revision 3.5.

3.16.17.2 Measurement requirements

The required measurements are:
a) see Section 7.6.23 of Serial ATA Revision 3.5 for detailed descriptions of this requirement;
b) this test requirement is only applicable to products running at the 6 Gbps interface rate;
c) testing of this requirement is limited to the differential of the High Frequency Test Pattern (HFTP);
d) a method to measure the common mode voltage is attaching a metrology-grade power combiner between the Tx+ and Tx- outputs of the transmitter, at the Device or Host transmit connector. Both outputs shall be joined to the combiner with phase matched cables having ≤ ± 3 ps of mismatch, diminishing phase distortion during the measurement;
e) the power combiner's output, or equivalent output method, is connected to an instrument capable of measuring spectral content with sufficient bandwidth to measure the fundamental and second harmonic frequencies of the data rate (i.e., 6 Gbps, fundamental = 3 GHz);

f) the measurement shall be made using a 1 MHz resolution bandwidth;
g) the spectral windowing function shall use a Gaussian window; and
h) the dBmV level is understood to be 0 dBmV = 1 mV into 50 ohm.

3.16.17.3 Pass/fail criteria

The Transmitter shall not deliver more output voltage than the following limits:
a) the fundamental (i.e., 3 GHz) shall be measured to be a maximum of 26 dBmV(pk); and
b) the second Harmonic (i.e., 6 GHz) shall be measured to be a maximum of 30 dBmV(pk).

3.16.18 TSG-17 : Gen3 (6 Gbps) Tx Emphasis

3.16.18.1 Device/host expected behavior

See Section 7.6.33 of Serial ATA Revision 3.5.

3.16.18.2 Measurement requirements

The required measurements are:
a) see Section 7.4.3.3.14 of Serial ATA Revision 3.5 for detailed descriptions of this requirement;
b) this test requirement is only applicable to products running at the 6 Gbps interface rate. Note, emphasis is defined for Gen1 and Gen2 but is informative and not described in this section;
c) the TX Emphasis requirement does not apply to devices using or mating with the following:
   A) internal LIF-SATA connector;
   B) SATA MicroSSD interface; or
   C) Internal M.2 connector;
d) the Tx Emphasis requirement does not apply to the Internal 4-lane cable mated to a backplane;
e) testing of this requirement uses the MFTP;
f) transmitter emphasis values specified in Table 54 and Table 55 updates in Serial ATA Revision 3.5. Refer to the output signal from the unit under test (UUT) at the mated connector of the device;
g) the CIC for the Tx Emphasis measurements is required for Gen3i internal 1 m cabled host to device applications per Section 7.4.3.3.14 of Serial ATA Revision 3.5; and
h) the $V_{EmphasisDevice}$ and $V_{EmphasisHost}$ measurements shall be calculated using the procedure outlined in Section 7.6.33 of Serial ATA Revision 3.5.

3.16.18.3 Pass/fail criteria

The Transmitter emphasis shall be within the limits shown in Table 11.

Parameter	Limit	Gen3i Emphasis (dB)	Gen3u Emphasis (dB)
$V_{EmphasisDevice}$ Device Tx Emphasis	Min	0.5	-
	Max	2.5	-
$V_{EmphasisHost}$ Host Tx Emphasis	Min	-2	-2
	Max	1.5	1.5

Table 11 – Transmitter emphasis

3.17 Phy receiver requirements

3.17.1 Overview

During the testing execution for all RX test requirements, it is essential that the product under test be able to complete an initial OOB sequence through the device COMWAKE. This is to allow product calibration to occur prior to and/or during the initial power on and detect sequences.

3.17.2 RX-01 : Pair differential impedance (informative)

3.17.2.1 Device/host expected behavior

See Section 7.4.3.4.2 of Serial ATA Revision 3.5.

3.17.2.2 Measurement requirements

a) see Section 7.6.15 and Section 7.6.28 of Serial ATA Revision 3.5;
b) this test requirement is only applicable to products that support a maximum operating speed of 1.5 Gbps. For products that support a maximum operating speed of 3 Gbps or 6 Gbps this test is not required; and
c) testing of this requirement shall be completed during a PHYRDY Interface Power State (see Section 8.1 of Serial ATA Revision 3.5). The amplitude of a TDR pulse or excitation applied to a receiver shall not exceed 300 mVpp (-6.48 dBm 50 ohm) single-ended.

3.17.2.3 Pass/Fail Criteria

The pass/fail requirements are:

a) verify that both the minimum [RX-01a] and maximum [RX-01b] results for the pair differential impedance measured between 85 ohm and 115 ohm (for products running at 1.5 Gbps); and
b) the verification of this result is conditional. If a product which supports 1.5 Gbps product passes RX-06, then it is not required that this test be verified. This result shall be verified for a 1.5 Gbps product if it fails RX-06.

3.17.3 RX-02 : Single-ended impedance (obsolete)

3.17.3.1 Device/host expected behavior

See Section 7.4.3.2.3 of Serial ATA Revision 3.5.

3.17.3.2 Measurement requirements

The required measurements are:

a) see Section 7.6.15 and 7.6.29 of Serial ATA Revision 3.5;
b) this test requirement is only applicable to products that support a maximum operating speed of 1.5 Gbps. For products that support a maximum operating speed of 3 Gbps or 6 Gbps this test is not required; and
c) testing of this requirement shall be completed during a PHYRDY Interface Power State (see Section 8.1 of Serial ATA Revision 3.5). The amplitude of a TDR pulse or excitation applied to a receiver shall not exceed 300 mVpp (-6.48 dBm 50 ohm) single-ended.

3.17.3.3 Pass/fail criteria

The pass/fail requirements are:

a) $Z_{s\text{-}eRX}$ measured to be at least 40 ohm (for products running at 1.5 Gbps); and
b) both the minimum [RX-02a] and the maximum [RX-02b] results shall be captured.

3.17.4 RX-03 : Gen2 (3 Gbps) Differential mode return loss (informative)

3.17.4.1 Device/host expected behavior

See Section 7.4.3.4.4, Section 7.4.3.2.4, and Section 7.4.3.2.7 of Serial ATA Revision 3.5.

3.17.4.2 Measurement requirements

The required measurements are:

a) see Section 7.6.15 of Serial ATA Revision 3.5;
b) calibrate to the end of the SMA cables, but do *not* include (i.e., de-embed) the SMA to SATA PCB and the SATA connector, so the board and the SATA connector are *included* with the product measurement;
c) this test requirement is only applicable to products that support a maximum operating speed of 3 Gbps. For products that support a maximum operating speed of 1.5 Gbps or 6 Gbps this test is not required; and
d) testing of this requirement shall be completed during a PHYRDY Interface Power State (see Section 8.1 of Serial ATA Revision 3.5). The amplitude of a TDR pulse or excitation applied to a receiver shall not exceed 300 mVpp (-6.48 dBm 50 ohm) single-ended.

3.17.4.3 Pass/fail criteria

The $RL_{DD11,RX}$ is measured per the values in 7.4.3.4.4, 7.4.3.2.4, and 7.4.3.2.7 of Serial ATA Revision 3.5 for products running at 3 Gbps.

Test Name	Frequency	Minimum (dB)
RX-03a	150 MHz to 300 MHz	18
RX-03b	300 MHz to 600 MHz	14
RX-03c	600 MHz to 1.2 GHz	10
RX-03d	1.2 GHz to 2.4 GHz	8
RX-03e	2.4 GHz to 3 GHz	3
RX-03f	3 GHz to 5 GHz	1 (na for Gen2m)

Table 12 – RX Differential Mode Return Loss

3.17.5 RX-04 : Gen2 (3 Gbps) common mode return loss (informative)

3.17.5.1 Device/host expected behavior

See Section 7.4.3.4.5 of Serial ATA Revision 3.5.

3.17.5.2 Measurement requirements

The required measurements are:

a) see Section 7.6.15 of Serial ATA Revision 3.5;
b) calibrate to the end of the SMA cables, but do *not* include (de-embed) the SMA to SATA PCB and the SATA connector, so the board and the SATA connector are *included* with the product measurement;
c) this test requirement is only applicable to products that support a maximum operating speed of 3.0 Gbps. For products that support a maximum operating speed of 1.5 Gbps or 6.0 Gbps this test is not require; and
d) testing of this requirement shall be completed during a PHYRDY Interface Power State (see Section 8.1 of Serial ATA Revision 3.5). The amplitude of a TDR pulse or excitation applied to a receiver shall not exceed 300 mVpp (-6.48 dBm 50 ohm) single-ended.

3.17.5.3 Pass/fail criteria

The $RL_{CC11,RX}$ is measured per the values in 7.4.3.4.5 of Serial ATA Revision 3.5 for products running at 3 Gbps.

Test Name	Frequency	Minimum (dB)
RX-04a	150 MHz to 300 MHz	5
RX-04b	300 MHz to 600 MHz	5
RX-04c	600 MHz to 1.2 GHz	2
RX-04d	1.2 GHz to 2.4 GHz	1
RX-04e	2.4 GHz to 3 GHz	1
RX-04f	3 GHz to 5 GHz	1 (na for Gen2m)

Table 13 - RX Common Mode Return Loss

3.17.6 RX-05 : Gen2 (3 Gbps) Impedance balance (informative)

3.17.6.1 Device/host expected behavior

See Section 7.4.3.4.6 of Serial ATA Revision 3.5.

3.17.6.2 Measurement requirements

The required measurements are:

a) see Section 7.6.15 of Serial ATA Revision 3.5;
b) this test requirement is only applicable to products that support a maximum operating speed of 3 Gbps. For products that support a maximum operating speed of 1.5 Gbps or 6 Gbps this test is not required; and
c) testing of this requirement shall be completed during a PHYRDY Interface Power State (see Section 8.1 of Serial ATA Revision 3.5). The amplitude of a TDR pulse or excitation applied to a receiver shall not exceed 300 mVpp (-6.48 dBm 50 ohm) single-ended.

3.17.6.3 Pass/fail criteria

The $RL_{DC11,RX}$ is measured per the values in Section 7.4.3.4.6 of Serial ATA Revision 3.5 for products running at 3 Gbps.

Test Name	Frequency	Minimum (dB)
RX-05a	150 MHz to 300 MHz	30
RX-05b	300 MHz to 600 MHz	30
RX-05c	600 MHz to 1.2 GHz	20
RX-05d	1.2 GHz to 2.4 GHz	10
RX-05e	2.4 GHz to 3 GHz	4
RX-05f	3 GHz to 5 GHz	4 (na for test Gen2m)

Table 14 -RX Impedance Balance

3.17.7 RX-06 : Gen1 (1.5 Gbps) differential mode return loss (informative)

3.17.7.1 Device/host expected behavior

See Section 7.4.3.4.4 of Serial ATA Revision 3.5.

3.17.7.2 Measurement requirements

The required measurements are:

a) see Section 7.6.15 of Serial ATA Revision 3.5;
b) calibrate to the end of the SMA cables, but do *not* include (de-embed) the SMA to SATA PCB and the SATA connector, so the board and the SATA connector are *included* with the product measurement;

c) this test requirement is only applicable to products that support a maximum operating speed of 3 Gbps. For products that support a maximum operating speed of 1.5 Gbps or 6 Gbps this test is not required; and
d) testing of this requirement shall be completed during a PHYRDY Interface Power State (see Section 8.1 of Serial ATA Revision 3.5). The amplitude of a TDR pulse or excitation applied to a receiver shall not exceed 300 mVpp (-6.48 dBm 50 ohm) single-ended.

3.17.7.3 Pass/fail criteria

The $RL_{DD11,RX}$ is measured per the values in TSG-14 for Gen3 for product running at 1.5 Gbps.

Test Name	Frequency	Minimum (dB)
RX-06a	75 MHz to 150 MHz	18
RX-06b	150 MHz to 300 MHz	14
RX-06c	300 MHz to 600 MHz	10
RX-06d	600 MHz to 1.2 GHz	8
RX-06e	1.2 GHz to 2.4 GHz	3
RX-06f	2.4 GHz to 3 GHz	1 (na for Gen1m)

Table 15 - RX Differential Mode Return Loss for 1.5 Gbps

3.17.8 RX-07 : Gen3 (6 Gbps) differential mode return loss (informative)

3.17.8.1 Device/host expected behavior

See Section 7.4.3.2.7 of Serial ATA Revision 3.5.

3.17.8.2 Measurement requirements

The required measurements are:
a) see Section 7.6.15 of Serial ATA Revision 3.5;
b) calibrate to the end of the SMA cables, but do *not* include (i.e., de-embed) the SMA to SATA PCB and the SATA connector, so the board and the SATA connector are *included* with the product measurement;
c) this test requirement is only applicable to products that support a maximum operating speed of 6 Gbps. For products that support a maximum operating speed of 1.5 Gbps or 3 Gbps, this test is not required; and
d) testing of this requirement shall be completed during a PHYRDY Interface Power State (see Section 8.1 of Serial ATA Revision 3.5). The amplitude of a TDR pulse or excitation applied to a receiver shall not exceed 300 mVpp (-6.48 dBm 50 ohm) single-ended.

3.17.8.3 Pass/fail criteria

The pass/fail requirements are:
a) $RL_{DD11,TX}$ measured per the values in Section 7.4.3.2.7 of Serial ATA Revision 3.5 for products running at 6 Gbps; and
b) the Return loss limit line starts at 300 MHz at -18 dB increasing at 13 dB/decade to 6 GHz.

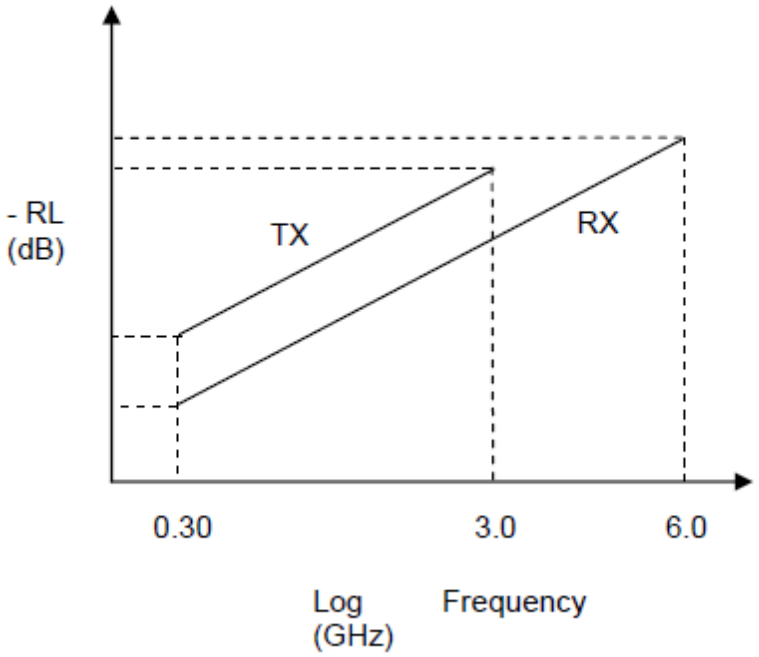


Figure 16- RX Differential Mode Return Loss for 6 Gbps

3.17.9 RX-08 : Gen3 (6 Gbps) impedance balance (informative)

3.17.9.1 Device/host expected behavior

See Section 7.4.3.4.6 of Serial ATA Revision 3.5.

3.17.9.2 Measurement requirements

The required measurements are:

a) see Section 7.6.15 of Serial ATA Revision 3.5;
b) this test requirement is only applicable to products running at 6 Gbps;
c) this test requirement is only applicable to products that support a maximum operating speed of 6 Gbps. For products that support a maximum operating speed of 1.5 Gbps or 3 Gbps, this test is not required; and
d) testing of this requirement shall be completed during a PHYRDY Interface Power State (see Section 8.1 of Serial ATA Revision 3.5). The amplitude of a TDR pulse or excitation applied to a receiver shall not exceed 300 mVpp (-6.48 dBm 50 ohm) single-ended.

3.17.9.3 Pass/fail criteria

The $RL_{DC11,RX}$ is measured per the values in Section 7.4.3.4.6 of Serial ATA Revision 3.5 for products running at 6 Gbps.

Test Name	Frequency	Minimum (dB)
RX-08a	150 MHz to 300 MHz	30
RX-08b	300 MHz to 600 MHz	30
RX-08c	600 MHz to 1.2 GHz	20
RX-08d	1.2 GHz to 2.4 GHz	10
RX-08e	2.4 GHz to 3 GHz	10
RX-08f	3 GHz to 5 GHz	4
RX-08g	5 GHz to 6.5 GHz	4

Table 17 -RX Impedance Balance

3.18 Phy receive signal requirements

3.18.1 Overview

During the testing execution for all RSG test requirements, it is essential that the product under test be able to complete an initial OOB sequence through the device COMWAKE prior to transmission of a BIST FIS or initiation of the BIST mode sequence. This is to allow product calibration to occur prior to and/or during the initial power on and detect sequences.

> NOTE 53 - The intent of the receiver test is to stress test the PUT's receiver and integrated components to validate that the system is able to tolerate the prescribed impaired signals in line with Table 57 and Table 58 and Section 7.4.3.1.3 of the Serial ATA Revision 3.5. This implies that the stimulus causes the product under test to retime the pattern in loopback (i.e., a compliant test implementation causes that the occurrences of Aligns between the stimulus pattern and after loopback are not identical over complete test time). The MOIs for test equipment shall provide sufficient detail for covering this requirement for all RSG tests.

Products shall support BIST L at all supported data rates.

3.18.2 General RSG calibration requirements

Tester shall save all the calibration data (i.e., screen shot) that is done daily at a minimum, if not every device evaluation. Valid calibration data shall be available per product for review, even if the same calibration data (i.e., daily) is used for multiple products. It is required that calibration be completed for this area of testing to ensure consistent measurements and environment impacts.

The following drawing illustrates two different test points (TP1 and TP2) that shall be used for impaired signal calibrations. The reference plane for all calibrations is the end of the 50 ohm SMA or equivalent cables at TP1 or TP2. The channel introduces inter-symbol interference (ISI).

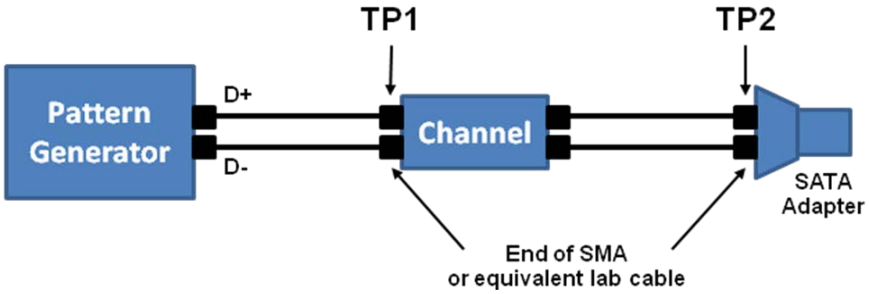


Figure 18 – Test points for RSG setup calibration.

The following parameters shall be used for creating the appropriate input source involved in the RSG tests (see Table 57 and Table 58 of Serial ATA Revision 3.5 Specification for Specification requirements):

a) pre-emphasis of 0 dB; and
b) no Clock Data Recover (CDR) unit to be used for the jitter calibration, explicit clock to be used (or equivalent). Real time scopes use a dataset derived clock, and BERTs use either a 1.5 GHz, 3 GHz, or 6 GHz square wave direct from the jitter source dependent on data rate. More details are available in MOIs.

The following table summarizes various calibrations that shall be referenced in later sections. In addition the table defines an order in which the calibrations have to be performed (i.e., steps 1 to 4).

The UTD covers a range of products and therefore the table lists a superset of calibrations. When testing a product only the calibrations are required which apply for that particular product.

Table 19 – RSG Setup Calibration Steps and Settings

Step		Test Point	Calibration Pattern	Method	Gen1i	Gen1m	Gen2i	Gen2m	Gen3i	Gen3u[a]
1	Rise/ Fall Time	TP1	LFTP	Section 7.6.6 in Serial ATA Revision 3.5	100 ps (20 % to 80 %)		100 ps (20 % to 80 %)		62 ps to 75 ps (20 % to 80 %)	
2	Rj	TP1	MFTP	Section 7.6.14 of Serial ATA Revision 3.5, Rj method also applied to Gen1i/m and Gen2i/m	8.57 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)		4.285 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)		2.14 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)	
3	Sj	TP1	MFTP	Using Rj method defined in Section 7.6.14 of Serial ATA Revision 3.5 for all data rates	Sj=270 mUI		Sj=270 mUI		Sj=192 mUI	
4	Tj	TP2	FCOMP with 2 Aligns and new LBP section	See UTD Section 3.18.4	Tj(min)=501 mUI Tj(max)=519 mUI Using a channel that introduces 40 ps ± 6 ps (i.e., min 34 ps and max 46 ps) of ISI in the given setup		Tj(min)=552 mUI Tj(max)=588 mUI Using a channel that introduces 40 ps ± 6 ps (i.e., min 34 ps and max 46 ps) of ISI in the given setup		Tj(min)=498 mUI Tj(max)=570 mUI Using a CIC that introduces a min 21 ps and max 33 ps of ISI in the given setup and that follows the definition in Section 7.4.8 of Serial ATA Revision 3.5	
5	Amplitude	TP2	FCOMP with 2 Aligns and new LBP section	For this test the amplitude distribution shall be either measured over a minimum 5×10^6 number of unit intervals at the 50 % location of the bit interval using previously calibrated edge rates and jitter. It is required to ensure that the maximum allowed voltage is not exceeded. Sections 7.6.4 and 7.6.14 of Serial ATA Revision 3.5	325 mV	240 mV	275 mV	240 mV	240 mV (Host), 200 mV (Device) Maximum not to exceed peak to peak voltage 1 V	
					Maximum not to exceed peak to peak voltage 600 mV		Maximum not to exceed peak to peak voltage 750 mV			

[a] Gen3u lab-sourced signals for minimum RX Differential Input Voltage and TJ are adjusted using the Gen3i CIC into a lab-load. After setting these levels the Gen3i CIC is removed and the resulting signal is applied to the UHost receiver under test. Devices shall use the CIC channel; this exception is only made for UHosts.

[b] All measurements in this table are to be performed with an explicit clock or equivalent.

3.18.2.1 Tj measurement method

Rise/fall times, Rj, and Sj are calibrated previously. Ensure that the channel in the calibration setup generates the specified amount of ISI. For Gen3i additionally the CIC requirements apply as defined in Section 7.4.8 of Serial ATA Revision 3.5.

Informative statement on ISI measurements at TP2. For ISI measurements turn off all other jitter. Rise/fall times are calibrated previously. Dry run results show that DDJ readings from oscilloscopes correlate well with a calculated delta of a TJ measurement with MFTP and a TJ measurement with LBP on a BERT.

For each frequency f $\in$ {5 MHz, 10 MHz, 33 MHz, 62 MHz} ensure that the Tj measured at TP2 is within the required range. The methodology of obtaining the appropriate configuration shall follow Section 7.6.13 of Serial ATA Revision 3.5 for Gen1i/m and Gen2i/m and Section 7.6.14 for Gen3i of Serial ATA Revision 3.5. The Tj measurement shall be a clock to data measurement using a clean (i.e., jitter free) clock signal from the pattern generator.

3.18.3 RSG-01 : Gen1 (1.5 Gbps) receiver jitter tolerance test

3.18.3.1 Device/host expected behavior

See Section 7.4.3.5.8 and Section 7.5 of Serial ATA Revision 3.5.

3.18.3.2 Measurement requirements

The required measurements are:

a) see Section 7.6.11 of Serial ATA Revision 3.5. See parameter details and calibration procedure for Gen1i/m in 3.18.2 . The source amplitude shall be calibrated for Gen1i or Gen1m. This test requirement is applicable to all products. The data rate is 1.5 Gbps; and
b) the MOIs for test equipment shall provide sufficient detail for implementing the above high level procedure using specific test equipment.

3.18.3.3 Pass/fail criteria

The pass/fail requirements are:

a) test is run using the FCOMP pattern which contains 2 Aligns and the new LBP section for 10 min and verified to exhibit no more than zero frame errors for all four Sj frequencies:
   A) 10 MHz – RSG-01a;
   B) 33 MHz – RSG-01b;
   C) 62 MHz – RSG-01c; and
   D) 5 MHz – RSG-01d;
   and
b) in the case where at least 1 000 errors are observed during test execution, the test iteration may stop (i.e., test time < 10 min for a specific frequency due to high number of errors).

3.18.4 RSG-02 : Gen2 (3 Gbps) receiver jitter tolerance test

3.18.4.1 Device/host expected behavior

See Section 7.4.3.5.8 and Section 7.5 of Serial ATA Revision 3.5.

3.18.4.2 Measurement requirements

The required measurements are:

a) see Section 7.6.11 of Serial ATA Revision 3.5. See parameter detail and calibration procedure for Gen2i/m in Section 3.18.2 . The source amplitude shall be calibrated for Gen2i or Gen2m;
b) this test requirement is only applicable to products claiming ability to run at 3 Gbps or 6 Gbps;
c) the data rate is 3 Gbps; and
d) the MOIs for test equipment shall provide sufficient detail for implementing the above high level procedure using specific test equipment.

3.18.4.3 Pass/fail criteria

The required measurements are:

a) test is run using the FCOMP pattern with 2 Aligns and new LBP section for 5 min and verified to exhibit no more than zero frame errors all four Sj frequencies:
   A) 10 MHz – RSG-02a;
   B) 33 MHz – RSG-02b;
   C) 62 MHz – RSG-02c; and
   D) 5 MHz – RSG-02d;
   and
b) in the case where at least 1 000 errors are observed during test execution, the test iteration may stop (i.e., test time < 5 min for a specific frequency due to high number of errors).

3.18.5 RSG-03 : Gen3 (6 Gbps) receiver jitter tolerance test

3.18.5.1 Device/host expected behavior

See Section 7.4.3.5.9 and Section 7.5 of Serial ATA Revision 3.5.

3.18.5.2 Measurement requirements

The required measurements are:

a) see Section 7.6.14 of Serial ATA Revision 3.5. See parameter detail and calibration procedure for Gen3 in 3.18.2 ;
b) this test requirement is only applicable to products claiming the ability to run at 6 Gbps. The data rate is 6 Gbps; and
c) the methods of implementation for test equipment shall provide sufficient detail for implementing the above high level procedure using specific test equipment.

3.18.5.3 Pass/fail criteria

The pass/fail requirements are:

a) test is run using the FCOMP pattern with 2 Aligns and new LBP section for 2 min and 30 s and verified to exhibit no more than zero frame errors all four Sj frequencies:
   A) 10 MHz – RSG-03a;
   B) 33 MHz – RSG-03b;
   C) 62 MHz – RSG-03c; and
   D) 5 MHz – RSG-03d;
   and
b) in the case where at least 1 000 errors are observed during test execution, the test iteration may stop (i.e., test time < 2 min and 30 s for a specific frequency due to high number of errors).

3.18.6 RSG-04 : Reserved place holder

Reserved place holder.

3.18.7 RSG-05 : Receiver stress test at +350 ppm

3.18.7.1 Device/host expected behavior

See Section 7.4.3.5.8, and Section 7.5 of Serial ATA Revision 3.5.

3.18.7.2 Measurement requirements

The required measurements are:

a) see Section 7.6.13 of Serial ATA Revision 3.5. See parameter detail and calibration procedure for Gen1i/m in Section 3.18.2 . The test is performed with all impaired signal conditions defined for Gen1i/m including Rj, Sj, ISI, and Sj frequency is 62 MHz. The source amplitude shall be calibrated for Gen1i or Gen1m;
b) this test requirement is applicable to all products. The data rate of the pattern generator is 1.5 Gbps increased by an additional 350 ppm; and

c) the methods of implementation for test equipment shall provide sufficient detail for implementing the above high level procedure using specific test equipment.

3.18.7.3 Pass/fail criteria

The pass/fail requirements are:

a) test is run using the framed COMP pattern with 2 Aligns and new LBP section over a minimum of 18 successive iterations of the framed COMP pattern with 2 Aligns and new LBP section and verified to exhibit no more than zero frame errors. The pattern generator shall run asynchronously to the product under test; and
b) if the test is conducted over more than 18 successive iterations of the framed COMP pattern with an observed frame error rate no greater than 8.2×10^{-8} (reference Section 7.6.3.3 of the Serial ATA Revision 3.5), the test is passed.

3.18.8 RSG-06 : Receiver stress test with SSC (informative)

3.18.8.1 Device/host expected behavior

See Section 7.4.3.1.6, Section 7.4.3.1.7, Section 7.4.3.5.8, and Section 7.5 of Serial ATA Revision 3.5.

Intent of test, running with SSC at Gen1 rates is considered suitably stressful and eliminates the duplicity of tests at higher data rates.

3.18.8.2 Measurement requirements

The required measurements are:

a) see Section 7.6.13 of Serial ATA Revision 3.5. See parameter detail and calibration procedure for Gen1i/m in Section 3.18.2 . The test is performed with all impaired signal conditions defined for Gen1i/m including Rj, Sj, ISI, and Sj frequency is 62 MHz. The source amplitude shall be calibrated for Gen1i or Gen1m;
b) this test requirement is applicable to all products. The data rate of the pattern generator is 1.5 Gbps reduced by an additional 350 ppm with an ideal 5 000 ppm triangular downspread spread spectrum clock (SSC) at 33 kHz modulation frequency (i.e., the data rate range is between 1.5 Gbps reduced by an additional 5 350 ppm and 1.5 Gbps reduced by an additional 350 ppm);
c) the methods of implementation for test equipment shall provide sufficient detail for implementing the above high level procedure using specific test equipment; and
d) in the presence of SSC, the base jitter parameters as defined is Table 15 should change no more than 10 %.

3.18.8.3 Pass/fail criteria

The pass/fail requirements are:

a) test is run using the framed COMP pattern with 2 Aligns and new LBP section over a minimum of 18 successive iterations of the framed COMP pattern with 2 Aligns and new LBP section and verified to exhibit no more than zero frame errors. The pattern generator shall run asynchronously to the product under test; and
b) if the test is conducted over more than 18 successive iterations of the framed COMP pattern with an observed frame error rate no greater than 8.2×10^{-8} (reference Section 7.6.3.3 of Serial ATA Revision 3.5), the test is passed.

3.19 Phy OOB requirements

3.19.1 Overview

Min and max pulse and gap widths shall consider both the +100 mV and the -100 mV edges for determining starting and ending times.

3.19.2 OOB-01 : OOB signal detection threshold

3.19.2.1 Device/host expected behavior

See Section 7.4.3.6.3 of Serial ATA Revision 3.5.

3.19.2.2 Measurement requirements

The required measurements are:

a) see Section 7.6.26 of Serial ATA Revision 3.5;
b) note that the Specification stipulates a Detection Threshold with value of V_{thresh}, where V_{thresh} is 50 mV ≤ V_{thresh} ≤ 200 mV for 1.5 Gbps products, and where V_{thresh} is 75 mV ≤ V_{thresh} ≤ 200 mV for 3 Gbps and 6 Gbps products. For the interests of the Interoperability Program, the measurements shall only be taken to verify this requirement at the lower and upper limits. The signal amplitude level of the source generator shall be validated using a mode voltage measurement at 0.45 UI to 0.55 UI;
c) to run this test on a device which supports a maximum data rate of 1.5 Gbps (i.e., Gen 1 only), a COMINIT/COMRESET burst is issued to the product at the following voltage threshold limits:
   A) OOB-01a - 40 mV (at this limit, the product is expected to *not* detect the OOB signaling); and
   B) OOB-01b - 210 mV (at this limit, the product is expected to detect the OOB signaling);
d) to run this test on a device which supports a maximum data rate of 3 Gbps or 6 Gbps, a COMINIT/COMRESET burst is issued to the product at the following voltage threshold limits:
   A) OOB-01c - 60 mV (at this limit, the product is expected to *not* detect the OOB signaling); and

      NOTE 54 - Tool resolution preference is even values, as opposed to 75 mV.

   B) OOB-01d - 210 mV (at this limit, the product is expected to detect the OOB signaling);
e) in a case where a device supports Asynchronous Signal Recovery, it is possible that a device may transmit COMINIT pro-actively and not in direct response to a COMRESET. In verification of this test requirement, it is essential that the tester be able to extract any COMINIT response which may be as a result of Asynchronous Signal Recovery, and simply verify COMINIT responses as a result of COMRESET receipt from the host;
f) suggested test methodology requires sending the following test sequence continuously from a suitable generator;

      EXAMPLE: 6 × ((COMINIT/COMRESET burst + 480 UI_{OOB} gap) + 1) × (45 000 UI_{OOB} gap)

g) using a suitable instrument (e.g., real-time scope or equivalent) to observe a minimum continuous 2 ms window, verify that the PUT consistently responds to each COMINIT/COMRESET burst;
h) detection tests, changing the COMINIT/COMRESET burst amplitude values only, verify that the PUT continues to consistently respond to a COMINIT/COMRESET Burst amplitude value of 210 mV; and
i) No-Detection Tests: Changing the COMINIT/COMRESET burst amplitude values only, verify that the PUT consistently DOES *not* respond to a COMINIT/COMRESET burst amplitude value of 40 mV for 1.5 Gbps products (60 mV for 3 Gbps and 6 Gbps products), *with the exception of unsolicited COMINIT bursts due to ASR (see item e above)*.

3.19.2.3 Pass/fail criteria

The pass/fail requirements are:

a) for products with a maximum data rate of 1.5 Gbps:
   A) OOB-01a - Verification of no product COMINIT/COMRESET detection at 40 mV;
   B) OOB-01b - Verification of product COMINIT/COMRESET detection at 210 mV; and
   C) if any of the above cases fails, this is considered a failure by the product;
   or
b) for products with a maximum data rate of 3 Gbps or 6 Gbps:
   A) OOB-01c - Verification of no product COMINIT/COMRESET detection at 60 mV;
   B) OOB-01d - Verification of product COMINIT/COMRESET detection at 210 mV; and

C) if any of the above cases fails, this is considered a failure by the product.

3.19.3 OOB-02 : UI during OOB signaling

3.19.3.1 Device/host expected behavior

See Section 7.4.3.6.4 of Serial ATA Revision 3.5.

3.19.3.2 Pass/fail criteria

Mean UI_{OOB} measured to be between 646.67 ps and 686.67 ps over entire OOB burst.

3.19.4 OOB-03 : COMINIT/RESET and COMWAKE transmit burst length

3.19.4.1 Device/host expected behavior

See Section 7.4.3.6.5 of Serial ATA Revision 3.5.

3.19.4.2 Measurement requirements

The required measurements are:

a) see Section 7.6.27 of Serial ATA Revision 3.5;
b) this test is only run once at the maximum interface rate of the product (1.5 Gbps, 3 Gbps, or 6 Gbps);
c) note that the requirement within the Specification is called out in UI. For the interests of the Interoperability Program, the measured value (T) shall be compared against the minimum and maximum values of a multiple of UI_{OOB} in nanoseconds, where 103.5 ns ≤ T ≤ 110.9 ns (+1 % Larger than Spec Limit). The values above are obtained from the following formulas:
   A) Min (160) = 646.67 ps (Min UIoob) × 160 = 103.5 ns; and
   B) Max (160) = 686.67 ps (+1 %) (Max UIoob) × 160 = 110.9 ns (Note: +1 % on OOB is what gets measured, which requires a 4 % margin rather than the current specified 3 % margin); and
d) a minimum of 5 COMINIT/RESET and 5 COMWAKE bursts shall be captured and the mean of all captured values shall be reported.

3.19.4.3 Pass/fail criteria

Burst Length measured to be between minimum and maximum values of UI_{OOB} multiplied by 160 and reported in nanoseconds.

3.19.5 OOB-04 : COMINIT/RESET transmit gap length

3.19.5.1 Device/host expected behavior

See Section 7.4.3.6.7 of Serial ATA Revision 3.5.

3.19.5.2 Measurement requirements

The required measurements are:

a) see Section 7.6.27 of Serial ATA Revision 3.5;
b) this test is only run once at the maximum interface rate of the product (1.5 Gbps, 3 Gbps, or 6 Gbps);
c) note that the requirement within the Specification is called out in UI. For the interests of the Interoperability Program, the measured value (T) shall be compared against the minimum and maximum values of a multiple of UI_{OOB} in nanoseconds, where 310.4 ns ≤ T ≤ 329.6 ns. The values above are obtained from the following formulas:
   A) Min (480) = 646.67 ps (Min UIoob) × 480 = 310.4 ns; and
   B) Max (480) = 686.67 ps (Max UIoob) × 480 = 329.6 ns;
   and
d) per definition, devices shall be validated against the COMINIT Transmit Gap Length and hosts shall be verified against the COMRESET Transmit Gap Length. The requirement is the same in both cases.

3.19.5.3 Pass/fail criteria

Gap Length measured to be between minimum and maximum values of UI_{OOB} multiplied by 480 and reported in nanoseconds.

3.19.6 OOB-05 : COMWAKE transmit gap length

3.19.6.1 Device/host expected behavior

See Section 7.4.3.6.7 of Serial ATA Revision 3.5.

3.19.6.2 Measurement requirements

The required measurements are:

a) see Section 7.6.27 of Serial ATA Revision 3.5;
b) this test is only run once at the maximum interface rate of the product; and
c) the requirement within the Specification is called out in UI. For the interests of the Interoperability Program, the measured value (T) shall be compared against the minimum and maximum values of a multiple of UI_{OOB} in nanoseconds, where 102.4 ns (-1 % smaller than Spec Limit) ≤ T ≤ 109.9 ns. The values above are obtained from the following formulas:
   A) Min (160) = 646.67 ps (-1 %) (Min UIoob) × 160 = 102.4 ns; and
   B) Max (160) = 686.67 ps (Max UIoob) × 160 = 109.9 ns.

3.19.6.3 Pass/fail criteria

Gap Length measured to be between minimum and maximum values of UI_{OOB} multiplied by 160 and reported in nanoseconds.

3.19.7 OOB-06 : COMWAKE gap detection windows

3.19.7.1 Device/host expected behavior

See Section 7.4.3.6.8 of Serial ATA Revision 3.5.

3.19.7.2 Measurement requirements

The measurement requirements are:

a) see Section 7.6.27 of Serial ATA Revision 3.5;
b) this test is only run once at the maximum interface rate of the product;
c) note that the Specification stipulates a Detection Window with value of T, where T is 35 ns ≤ T < 175 ns. For the interests of the Interoperability Program, the measurements shall only be taken to verify this requirement at the lower and upper limits;
d) to run this test, a COMWAKE is issued to the product at the following limits:
   A) 153 UI_{OOB} (at this limit, the product is expected to respond with COMWAKE);
   B) 167 UI_{OOB} (at this limit, the product is expected to respond with COMWAKE);
   C) 45 UI_{OOB} (at this limit, the product is expected to *not* respond with COMWAKE); and
   D) 266 UI_{OOB} (at this limit, the product is expected to *not* respond with COMWAKE);

   NOTE 55 - There is no timing requirement for how soon following a host COMWAKE which the device shall respond with a device COMWAKE, and vice versa. For test efficiency purposes, a tester is only required to wait for verification of device COMWAKE up to 100 ms following de-qualification of host COMWAKE, and vice versa.

e) suggested test methodology requires sending the following test sequence continuously from a suitable generator. One of two sequences may be used. The alternative sequence may be used when cross-talk is a problem:

   Original sequence for devices:

   6 × (COMINIT/COMRESET burst + 480 UI_{OOB} gap) +
   1 × (45 000 UI_{OOB} gap) +
   6 × (COMWAKE burst + 160 UI_{OOB} gap) +

1 × (130 000 UI_{OOB} gap)

Alternative sequence for devices:

6 × (COMINIT/COMRESET burst + 480 UI_{OOB} gap) +
1 × (45 000 UI_{OOB} gap) +
6 × (COMWAKE burst + 160 UI_{OOB} gap) +
1 × (1 920 UI_{OOB} gap) + (needs to be calculated)
1 × (129 920 UI_{OOB} D10.2)

For Hosts:

6 × (COMINIT burst + 480 UI_{OOB} gap) +
1 × (300 000 UI_{OOB} gap) +
6 × (COMWAKE burst + 160 UI_{OOB} gap) +
1 × (2 720 UI_{OOB} gap) +
1 × (129 826 UI_{OOB} ALIGNp)

f) using a suitable instrument (e.g., real-time scope or equivalent) to observe a minimum continuous 2 ms window, verify that the PUT consistently responds to each OOB sequence by entering speed negotiation accordingly. Figure 3 shows an example screen capture of typical PUT behavior for nominal COMINIT/COMRESET and COMWAKE gaps;

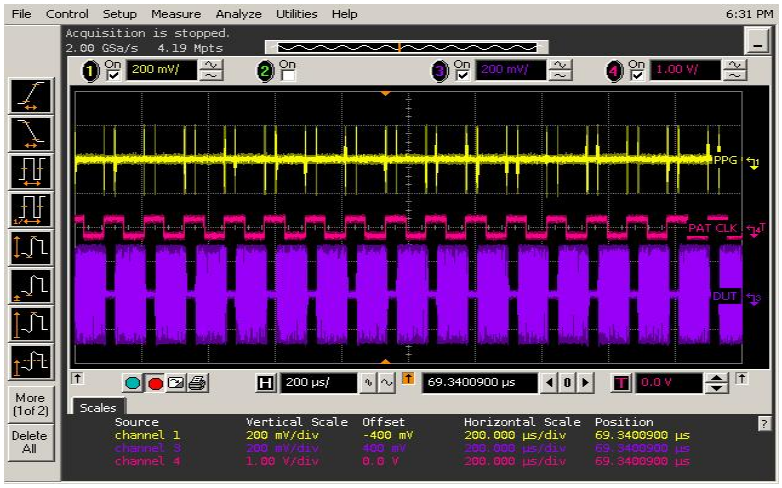


Figure 3 - Example OOB-06 test stimulus and PUT response, nominal COMINIT/COMRESET, COMWAKE
(Test stimulus top, yellow. PUT response bottom, purple.)

g) detection tests, changing the COMWAKE gap values only, verify that the PUT continues to consistently enter speed negotiation for gap values of 155 UI_{OOB} and 165 UI_{OOB} (103.33 ns and 110 ns, respectively);
h) no-detection tests, changing the COMWAKE gap values only, verify that the PUT consistently *does not* enter speed negotiation for gap values of 45 UI_{OOB} and 266 UI_{OOB} (30 ns and 177.33 ns, respectively). An example screenshot of typical PUT behavior appears in Figure 4 (note lack of speed negotiation sequence from PUT);

Figure 4 - Example OOB-06 test stimulus and PUT response for out-of-range COMWAKE (Test stimulus top, yellow. PUT response bottom, purple.)

and

i) a minimum of 5 COMINIT/RESET and 5 COMWAKE bursts shall be captured and the mean of all captured values shall be reported.

3.19.7.3 Pass/fail criteria

The pass/fail requirements are:

a) OOB-06a - COMWAKE shall respond at 155 UI_{OOB};
b) OOB-06b - COMWAKE shall respond at 165 UI_{OOB};
c) OOB-06c - COMWAKE shall not respond COMWAKE at 45 UI_{OOB};
d) OOB-06d - Verification of no product COMWAKE response at 266 UI_{OOB}; and
e) if any of the above cases fails, this is considered a failure by the product.

3.19.8 OOB-07 : COMINIT/COMRESET gap detection windows

3.19.8.1 Device/host expected behavior

See Section 7.4.3.6.9 of Serial ATA Revision 3.5.

3.19.8.2 Measurement requirements

The required measurements are:

a) see Section 7.6.27 of Serial ATA Revision 3.5;
b) this test is only run once at the maximum interface rate of the product;
c) note that the Specification stipulates a Detection Window with value of T, where T is 175 ns ≤ T < 525 ns. For the interests of the Interoperability Program, the measurements shall only be taken to verify this requirement at the lower and upper limits;
d) to run this test on a device, a COMRESET is issued to the device at the following limits:
   A) 459 UI_{OOB} (at this limit, the device is expected to respond with COMINIT);
   B) 501 UI_{OOB} (at this limit, the device is expected to respond with COMINIT);
   C) 259 UI_{OOB} (at this limit, the device is expected to *not* respond with COMINIT); and
   D) 791 UI_{OOB} (at this limit, the device is expected to *not* respond with COMINIT);

NOTE 56 - A device is required to respond by transmitting COMINIT within 10 ms of de-qualification of a received COMRESET signal (see Section 8.4.2 of Serial ATA Revision 3.5). With this in mind, a test only needs to wait up to 11 ms following de-qualification of COMRESET to ensure that the device is responding. If no COMINIT is received in this timeframe, this is considered a failure by the device to this test.

NOTE 57 - In a case where a device supports Asynchronous Signal Recovery, it is possible that a device may transmit COMINIT pro-actively and not in direct response to a COMRESET. In verification of this test requirement, it is essential that the tester be able to extract any COMINIT response which may be as a result of Asynchronous Signal Recovery, and simply verify COMINIT responses as a result of COMRESET receipt from the host.

e) to run this test on a host, a COMINIT is issued to the host at the following limits:
   A) 459 UI_{OOB} (at this limit, the host is expected to respond with COMWAKE);
   B) 501 UI_{OOB} (at this limit, the host is expected to respond with COMWAKE);
   C) 259 UI_{OOB} (at this limit, the host is expected to *not* respond with COMWAKE); and
   D) 791 UI_{OOB} (at this limit, the host is expected to *not* respond with COMWAKE);
f) suggested test methodology requires sending the following test sequence continuously from a suitable generator:

   For Device:

   6 × (COMINIT/COMRESET burst + 480 UI_{OOB} gap) +
   1 × (45 000 UI_{OOB} gap)

   For Host:

   6 × (COMINIT/COMRESET burst + 480 UI_{OOB} gap) +
   1 × (300 000 UI_{OOB} gap)

g) using a suitable instrument (e.g., real-time scope or equivalent) to observe a minimum continuous 2 ms window, verify that the PUT consistently responds to each COMINIT/COMRESET. Figure 5 shows a typical screen capture of proper PUT behavior for nominal COMINIT/COMRESET gaps;

Figure 5 - Example OOB-07 test stimulus and PUT response, for nominal COMINIT/COMRESET gap
(Test stimulus top, yellow. PUT response bottom, purple.)

h) detection tests, changing the COMINIT/COMRESET gap values only, verify that the PUT continues to respond to gap values of 459 UI_{OOB} and 501 UI_{OOB} (306 ns and 334 ns, respectively);
i) no-detection tests, changing the COMINIT/COMRESET gap values only, verify that the PUT consistently *does not* respond to gap values of 259 UI_{OOB} and 791 UI_{OOB} (172.66 ns and 527.3 ns, respectively), *with the exception of unsolicited COMINIT bursts due to ASR (see note above)*. An example screenshot of typical PUT behavior appears in Figure 6;

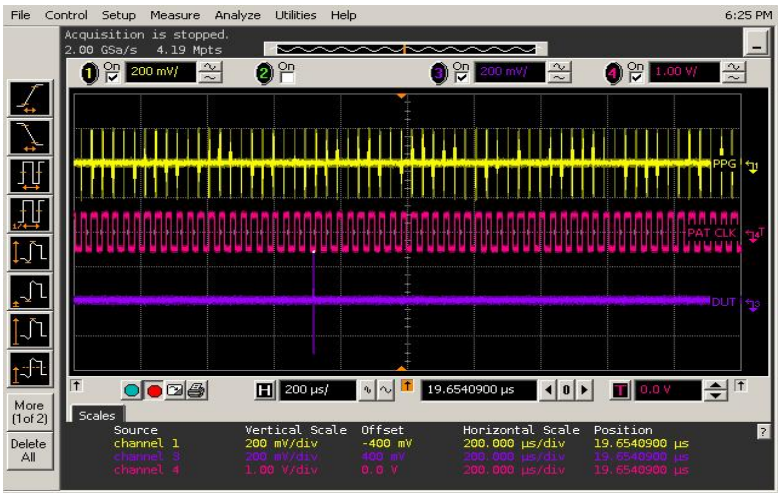


Figure 6 - Example OOB-07 test stimulus and PUT response for out-of-range COMINIT/COMRESET (Test stimulus top, yellow. PUT response bottom, purple.)

and

j) a minimum of 5 COMINIT/RESET and 5 COMWAKE bursts shall be captured and the mean of all captured values shall be reported.

3.19.8.3 Pass/fail criteria

The pass/fail requirements are:

a) device:
   A) OOB-07a - Verification of COMINIT response at 459 UI_{OOB};
   B) OOB-07b - Verification of COMINIT response at 501 UI_{OOB};
   C) OOB-07c - Verification of no COMINIT response at 259 UI_{OOB}; and
   D) OOB-07d - Verification of no COMINIT response at 791 UI_{OOB};
b) host:
   A) OOB-07a - Verification of COMWAKE response at 459 UI_{OOB};
   B) OOB-07b - Verification of COMWAKE response at 501 UI_{OOB};
   C) OOB-07c - Verification of no COMWAKE response at 259 UI_{OOB}; and
   D) OOB-07d - Verification of no COMWAKE response at 791 UI_{OOB};
   and
c) if any of the above cases fails, this is considered a failure by the product.

3.20 Port multiplier requirements (informative)

3.20.1 Overview

Devices used for testing Port Multipliers shall be limited to HDD type devices.

All tests in this Section are intended to be run in a configuration based on a Port Multiplier Aware Host. A Port Multiplier Aware Host is defined by the two following characteristics:

a) a hardware platform in which at least one HBA (resident in the motherboard chipset or on a separate PCB) is capable of using non-zero values in the PM Port field in the FISes it sends and receives; and
b) an OS and OS device driver which shall discover and enumerate any attached port multipliers during system initialization.

3.20.2 PM-01 : Device Port 0 enabled by default

3.20.2.1 Expected behavior

See Section 16.2 and Section 16.3.3.3 of Serial ATA Revision 3.5.

Serial ATA Revision 3.5 requires that a host system that has no explicit support for Port Multipliers (PM) shall work with a device connected to PM device Port 0. In this configuration the PM is transparent to both host and device, with the exception of time required for a transmission from one end device to the other.

More specifically, a host system should be able to issue Soft Reset and all the commands used during a boot sequence to a device attached to PM Port 0, with results identical to those obtained when the same device is directly attached to a SATA HBA.

For this document we shall run a series of representative commands. We shall not actually boot a system in this test. Port Booting a non-PM aware system from a Port Multiplier Port 0 device shall be a part of the testing.

3.20.2.2 Measurement requirements

The required measurements are:

1) attach a SATA HDD to Port 0 of the PM;
2) apply power to the PM, the drive, and the host system;
3) to emulate host system that has no explicit support for Port Multipliers, issue Soft Reset to Port 0 of the port multiplier before starting the test sequence; and
4) run the following ATA commands as defined in ACS-4:
    1) IDENTIFY DEVICE;
    2) SET FEATURES with Features Register = 02h (Enable Write Cache) or a similarly benign Feature Register value;
    3) WRITE DMA with one sector of nonzero data to LBA 0; and
    4) READ DMA from LBA 0.

3.20.2.3 Pass/fail criteria

The pass/fail requirements are:

1) a correct HDD Signature FIS (34h) is received following power on, before the soft reset is issued;
2) a correct HDD Signature FIS (34h) is received in response to the soft reset; and
3) all commands complete without error (e.g., data read from LBA 0 is compared to the data written with no miscompares).

3.20.3 PM-02 : General status and control register (GSCR) access

3.20.3.1 Expected behavior

See Section 16.4.2 of Serial ATA Revision 3.5.

The GSCRs are accessed using the READ PORT MULTIPLIER and WRITE PORT MULTIPLIER commands with the PortNum field in the FIS27h Device field set to 15. The full range of register numbers addressable through these commands is 0 to 65 535, however most are Reserved and only a handful are Mandatory. We use the Mandatory registers to verify that the GSCRs is able to be accessed.

Table 20 - Mandatory GSCRs

Register	Definition	Testable Contents
GSCR[0]	Product Identifier	None (contents are vendor specific).
GSCR[1]	Revision Information	Bits [7:4, 31:16] reserved, shall be cleared to zero. Bits [3:1] spec support level, at least one bit shall be set to one. Bit [0] shall be cleared to zero.
GSCR[2]	Port Information	Bits [31:4] reserved, shall be cleared to zero. Bits [3:0] number of exposed ports, shall contain some value from 1 to 15.
GSCR[32]	Error Information	Bits [31:15] reserved, shall be cleared to zero.
GSCR[33]	Error Information Bit Enable	Default value = 0400 FFFFh All bits may be set or cleared by WRITE PORT MULTIPLIER.
GSCR[64]	Features Supported	Bits [31:5] reserved, shall be cleared to zero. Bits [4:0] indicate features supported, not predictable.
GSCR[96]	Features Enabled	Bits [31:4] reserved, shall be cleared to zero. Bits [3:0] indicate features enabled. After power on, bits 0 and 2 shall be the same as bits 0 and 2 in GSCR[64]. After power on, bits 1 and 3 shall be cleared to zero.

3.20.3.2 Measurement requirements

The required measurements are:

1) for setup consistency, issue Soft Reset to Port F of the port multiplier before starting the test sequence;
2) read each 32-bit register in Table 20. The information in these registers should be formatted and displayed on the test output device;
3) write all ones to GSCR[33], then read back and check the contents; and
4) write all zeros to GSCR[33], then read back and check the contents. Restore the default contents of the register.

3.20.3.3 Pass/fail criteria

The pass/fail requirements are:

1) Port Multiplier Signature FIS returned following the soft reset;
2) all READ PORT MULTIPLIER and WRITE PORT MULTIPLIER commands complete without error;
3) verify the contents of each register according to Table 20. Some fields are vendor specific or feature dependent and shall not be verified by this test; and
4) verify that all bits in GSCR[33] are able to be cleared to zero and set to one.

3.20.4 PM-03 : Port status and control register (PSCR) access

3.20.4.1 Expected behavior

See Section 16.4.2 and Section 14.2 of Serial ATA Revision 3.5.

Each device port in a Port Multiplier has a set of PSCRs associated with it. PSCRs are accessed using the READ PORT MULTIPLIER and WRITE PORT MULTIPLIER commands with the PortNum field in the FIS27h Device field set to the number of the port (range 0 to 14). The full range of register numbers addressable through these commands is 0 to 65 535, however most are Reserved and only three are Mandatory. We use the Mandatory registers to verify that the PSCRs are able to be accessed. The mandatory registers are defined identically to SATA SCR[0], SCR[1], and SCR[2] in a SATA HBA.

Table 21 - Mandatory PSCRs

Register	Definition	Testable Contents
PSCR[0]	SStatus	Bits [31:12] reserved, shall be cleared to zero. Bits [3:0] DET field, shall contain the value 4h following a Port Multiplier reset, except for device Port 0 on a non-PM aware host system.
PSCR[1]	SError	None in this test. Bits may be set as a consequence of device activity but the host shall not set bits, only clear them.
PSCR[2]	SControl	Bits [31:20] reserved, shall be cleared to zero. Bits [19:4] none in this test. Bits [3:0] DET field, shall contain the value 4h following a Port Multiplier reset, except for device Port 0 on a non-PM aware host system.

Caution, some port multipliers contain a SATA Enclosure Management Bridge (SEMB) that may be included in the count of exposed device ports in GSCR[2], bits [3:0]. For example, a port multiplier with 4 SATA device ports and 1 SEMB function could claim 5 ports in GSCR[2], bits [3:0]. Port 0 to Port 3 could be SATA device ports and Port 4 could be the SEMB.

In order to accurately determine the port configuration of a PM, the test is required to detect an SEMB or SATA port. This is able to be done by checking SStatus and a signature generated by the device. There are two possible signatures for an SEMB, depending on whether an SEP is connected to the SEMB. These signatures are defined in Section 13.14.4.2 of Serial ATA Revision 3.5. If an SEMB port is identified, that port shall not be selected for any of the PM tests defined in this document.

3.20.4.2 Measurement requirements

The required measurements are:

1) power cycle the port multiplier;
2) for setup consistency, issue Soft Reset to Port F of the port multiplier before starting the test sequence;
3) using bits [3:0] of GSCR[2], determine how many device ports the Port Multiplier under test contains. See note at end of this test description; and
4) connect a SATA device to one of the implemented device ports with a port number > 0. On the selected device port, write 0001b to the DET field (bits [3:0]) of PSCR[2], then write 0000b to the same location. This sequence requests that the port perform an interface communication initialization sequence, then progress to a PhyRdy state if a working device is attached.

3.20.4.3 Pass/fail criteria

The pass/fail requirements are:

1) all READ PORT MULTIPLIER and WRITE PORT MULTIPLIER commands shall complete without error;
2) verify that the reserved fields in each PSCR for all implemented ports except Port 0 contain all zeros. Verify that PSCR[2] bits [3:0] for all implemented ports except 0 contain 0100b; and
3) on the port with the attached SATA device, check the DET field in PSCR[0] and confirm that it contains 0011b. This confirms that communication has been established and indirectly confirms the two WRITE PORT MULTIPLIER were correctly processed.

NOTE 57 - It may be necessary to reset to zero the X bit in PSCR1 before a READ PORT MULTIPLIER to PSCR0 is expected to succeed.

3.20.5 PM-04 : 3 Gbps backwards compatibility

3.20.5.1 Expected behavior

See Section 17.5.7 of Serial ATA Revision 3.5.

If a device claims support for Serial ATA Gen2 signaling speed, 3 Gbps, (Word 76 bit 2 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data), then it shall also support Serial ATA Gen-1 signaling speed, 1.5 Gbps, (Word 76 bit 1 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data):

a) if the HBA supports only 1.5 Gbps signaling, then a 3 Gbps capable port multiplier shall negotiate for 1.5 Gbps operation on the host port. A compliant HBA is able to be forced to operate at Gen1-only speed through the SPD field of the SControl register in the HBA; or
b) if a device supports only 1.5 Gbps signaling, then a 3 Gbps capable port multiplier shall negotiate for 1.5 Gbps operation on the device port. There is not a standard way to force a Gen2 device to operate at Gen1-only speed. For this test it shall be necessary to either use a Gen1-only device or use a vendor unique method for restricting a Gen2 device to Gen1 speed.

3.20.5.2 Measurement requirements

The required measurements are:

1) for setup consistency, issue Soft Reset to Port F of the port multiplier before starting the test sequence; and
2) determine the native speed of the PM host interface by enabling the attached HBA port for Gen2 speed and observing the negotiated speed after a COMRESET sequence. If the PM is limited to Gen1 speed, then skip the rest of this test, as 3 Gbps backward compatibility does not apply:
    1) attach a port multiplier to a host SATA port that is restricted to 1.5 Gbps. Force a COMRESET sequence on the host SATA port; and
    2) attach a Gen1-only device to a port multiplier device port enabled for 3 Gbps operation. Force a COMRESET sequence on the device port.

3.20.5.3 Pass/fail criteria

The pass/fail requirements are:

1) observe in the HBA SStatus register that the interface is Active and the negotiated speed is 1.5 Gbps; and
2) observe in the PSCR SStatus register for the device port under test that the interface is Active and the negotiated speed is 1.5 Gbps.

3.20.6 PM-05 : Interface power management, H – PM, host initiated

3.20.6.1 Expected behavior

See Section 14.2 and Section 13.18 of Serial ATA Revision 3.5.

A port multiplier is required to respond to PMREQ_P and PMREQ_S on its host port with either PMACK or PMNAK. Actual support of the low power link states is optional. If a port multiplier responds to PMREQ_P and PMREQ_S on its host port with PMACK, then it is required to propagate the request to all active device ports.

3.20.6.2 Measurement requirements

The required measurements are:

1) for setup consistency, issue Soft Reset to Port F of the port multiplier before starting the test sequence;
2) determine whether low power modes are supported by the port multiplier:
    1) issue COMRESET from the HBA port to the host port of the PM and allow time for the sequence to complete;
    2) verify that the H-PM interface is in active state;
    3) issue PMREQ_P to the device using the SPM field of the HBA SPM register or through a vendor specific method;
    4) ensure that the H-PM interface goes to partial state;
    5) issue COMWAKE;
    6) ensure that the H-PM interface goes to active state;

7) if either of the above conditions are not met, put out a message, “Host – PM interface failed HIPM partial test.”;
8) issue PMREQ_S to the device using the SPM field of the HBA SPM register or through a vendor specific method;
9) ensure that the PM-Dev interface goes to slumber state;
10) issue COMWAKE and ensure that the PM-Dev interface goes to active state;
11) if either of the above conditions are not met, put out a message, “Host – PM interface failed HIPM slumber test.”; and
12) if the partial and slumber tests above are successful, proceed with testing or if they are not successful, put out a message, “Link low power states not supported by port multiplier.” and end test PM-05;

NOTE 59 - A host emulator/analyzer also may be used for these tests. Procedures are not documented here.

3) test whether PM propagates PMREQ to all active device ports:
   1) attach an HDD supporting HIPM to a device port;
   2) issue COMRESET to the PM host port and allow time for the sequence to complete;
   3) initialize the interface to the attached HDD;
   4) verify that the device port interface is active;
   5) issue PMREQ_P to the PM host port;
   6) read the IPM field in the SStatus register in the selected device port and record the state of the device port interface (sending a FIS27h with the READ PORT MULTIPLIER command should generate a COMWAKE on the H-PM interface to allow communicating with the PM, without awakening the PM-Dev interface); and
   7) repeat this procedure at step 1, starting with COMRESET then sending PMREQ_S instead of PMREQ_P;
4) measure PM partial state exit latency using the following steps:
   1) connect a bus analyzer to the H-PM interface;
   2) start the analyzer (optionally an oscilloscope or logic analyzer may be used instead);
   3) place the H-PM interface into partial state as described above;
   4) issue the COMWAKE OOB signal as described above;
   5) stop the bus analyzer or other device recording interface activity; and
   6) record the time between the end of the COMWAKE burst from the host to the end of the ALIGN burst following the COMWAKE burst from the PM;
5) measure PM slumber state exit latency using the following steps:
   1) connect a bus analyzer to the H-PM interface. Start the analyzer (optionally an oscilloscope or logic analyzer may be used instead);
   2) place the H-PM interface into partial state as described above;
   3) issue the COMWAKE OOB signal as described above;
   4) stop the bus analyzer or other device recording interface activity; and
   5) record the time between the end of the COMWAKE burst from the host to the end of the ALIGN burst following the COMWAKE burst from the PM;

   and
6) one execution of steps 1, 2, and 3 are required for this test. Ten iterations each of steps 4 and 5 above are required for this test.

3.20.6.3 Pass/fail criteria

The pass/fail requirements are:

1) determining whether low power modes are supported by the port multiplier is informative only, not subject to pass/fail evaluation but it may cause the rest of PM-05 to be skipped;
2) verify that the PM-Dev interface is in partial state following the first pass through this step and in slumber state following the second pass through this step. If both states are achieved, the test result is pass. If either state is incorrect, the test result is fail;
3) verify PM partial state exit latency for all steps is 10 us or less. If any time exceeds 10 us, then the result of this test is fail; and

4) verify that the PM slumber state exit latency times recorded for this step are all 10 ms or less. If any time exceeds 10 ms, then the result of this test step is fail.

3.20.7 PM-06 : Interface power management, H - PM, PM initiated

3.20.7.1 Expected behavior

See Section 14.2 and Section 13.18 of Serial ATA Revision 3.5.

A port multiplier may optionally support issuing power management requests to the host (PIPM) when all device ports are in a low power state or disabled. This capability, if supported, may be enabled or disabled by writing to bit 1 of GSCR[96]. There is no standard way to control which form of PMREQ is generated by a port multiplier.

There are three scenarios that will result in a PIPM request:

a) the last Active device port on the PM transitions to Disabled state as a result of the host writing 0100b to the DET field of the SControl register for that port;
b) the last Active device port on the PM transitions to Slumber or Partial state as the result of a HIPM request directed to the device on that port; or
c) a DIPM request from the device attached to the last Active device port on the PM.

3.20.7.2 Measurement requirements

The required measurements are:

1) for setup consistency, issue Soft Reset to Port F of the port multiplier before starting the test sequence;
2) attach and power up an HDD to a PM device port with a port number greater than zero;
3) verify that the port multiplier supports issuing PMREQ to the host;
4) issue COMRESET from the HBA port to the host port of the PM and allow time for the sequence to complete;
5) check PM GSCR[64] bit 1. If bit 1 is cleared to zero, then skip the rest of PM-06 and put out a message, “Port multiplier does not support issuing PMREQ to the host.”;
6) if bit 1 is set to one, then set PM GSCR[96] bit 1 is set to one;
7) verify that the PM then issue a PMREQ when one of the three scenarios described above occurs;
8) all device ports shall have been disabled by the COMRESET. This meets the requirement of scenario a) above;
9) wait 10 s. Check the state of the H-PM interface by reading the IPM field of the HBA SStatus register. If the interface is in partial or slumber state, continue to step 13 below;
10) if the H-PM interface is still in active state, then initialize the interface to the attached HDD. Issue PMREQ_S to the attached HDD. This is able to be done by writing first 0010b, then 0000b, to the SPM field of the device port SControl field;
11) wait 10 s;
12) check the state of the H-PM interface by reading the IPM field of the HBA SStatus register. If the interface is in partial or slumber state, continue to step 13 below;
13) if the H-PM interface is still in active state, check that the drive supports DIPM (IDENTIFY DEVICE Word 78 Bit 3), enable the DIPM feature in the drive using the SET FEATURES command and then issue a STANDBY IMMEDIATE command to the attached HDD;
14) wait 10 s. Check the state of the H-PM interface by reading the IPM field of the HBA SStatus register;
15) if the drive does not support DIPM or if none of these three scenarios has resulted in the H-PM interface entering partial or slumber state, put out a message for this subtest saying, “Unable to generate a port multiplier initiated partial or slumber state on the host – PM interface.” This condition shall be recorded as na, not fail; and
16) steps 13, 14, and 15 shall be repeated 10 times in sequence.

3.20.7.3 Pass/fail criteria

The pass/fail requirements are:

1) verify that the port multiplier supports issuing PMREQ to the host. Informative only, not subject to pass/fail evaluation. May cause the rest of PM-06 to be skipped; and
2) verify that the PM issues a PMREQ when one of the three scenarios described above occurs. If the H-PM interface enters partial or slumber state at least once, then the test result is pass. If the H-PM interface does not enter partial or slumber state at least once, then the test result is na.

3.20.8 PM-07 : Interface power management, PM - Dev, PM initiated

3.20.8.1 Expected behavior

See Section 13.18 of Serial ATA Revision 3.5.

On this interface the port multiplier device port is seen as a host port by the attached device. The device shall respond to IPM requests and to COMWAKE as if it were directly attached to an HBA.

3.20.8.2 Measurement requirements

The required measurements are:

1) for setup consistency, issue Soft Reset to Port F of the port multiplier before starting the test sequence;
2) verify that the device supports HIPM using the following steps:
    1) attach an HDD to the selected device port;
    2) initialize the PM-Dev interface. This can be done through the DET field of the SControl register of the device port;
    3) issue an IDENTIFY DEVICE command to the device;
    4) check IDENTIFY DEVICE word 76 bit 9. If bit 9 is set to one, then the device supports host (PM) initiated interface power management. Continue with the test; and
    5) if bit 9 is cleared to zero, then the device does not support HIPM. In that case, put out a message saying, “The device does not support HIPM.” Skip the remainder of this test;
3) verify correct PM-initiated IPM behavior on the selected device port using the following steps:
    1) initialize the PM-Dev interface. Ensure the interface is in the Active state;
    2) issue PMREQ_P to the device using the SPM field of the device port SPM register;
    3) ensure that the PM-Dev interface goes to partial state;
    4) issue COMWAKE and ensure that the PM-Dev interface goes to active state;
    5) if any of these conditions is not met, put out a message, “PM-Dev interface failed HIPM partial test.”;
    6) initialize the PM-Dev interface;
    7) ensure the interface is in the Active state;
    8) issue PMREQ_S to the device using the SPM field of the device port SPM register;
    9) verify that the PM-Dev interface goes to slumber state;
    10) issue COMWAKE and ensure that the PM-Dev interface goes to active state;
    11) if any of these conditions is not met, put out a message, “PM-Dev interface failed HIPM slumber test.”; and
    12) steps 5, 6, 7, and 8 shall be repeated 10 times.

3.20.8.3 Pass/fail criteria

The pass/fail requirements are:

1) verifying that the device supports HIPM is Informative only and not subject to pass/fail evaluation but it may cause the rest of PM-07 to be skipped;
2) verify correct PM-initiated IPM behavior on the selected device port; and
3) if the interface state is correct at each verification point in all 10 iterations of this test, then the result is pass. If the interface is in an incorrect state at any verification point during the 10 iterations of this test, then the result is fail.

3.20.9 PM-08 : Interface Power Management, PM - Dev, Dev Initiated

3.20.9.1 Expected behavior

See Section 13.18 of Serial ATA Revision 3.5.

Device initiated interface power management requests shall affect the PM-Dev link on which they are issued but shall not affect the interface power state of other device ports or the H-PM interface. There is no standard method to force a device to issue an IPM request, although devices with DIPM enabled shall generally do so within 10 s after receiving a STANDBY IMMEDIATE command.

3.20.9.2 Measurement requirements

The required measurements are:

a) for setup consistency, issue Soft Reset to Port F of the port multiplier before starting the test sequence;
b) verify that the device supports DIPM by using the following steps:
    1) connect an HDD to a device port in the port multiplier;
    2) initialize the PM-Dev interface for that port;
    3) verify that the interface is in active state;
    4) check that the drive supports DIPM (IDENTIFY DEVICE Word 78 Bit 3 is set to one);
    5) enable the DIPM feature in the drive using the SET FEATURES command;
    6) issue a STANDBY IMMEDIATE command to the attached HDD;
    7) wait 10 s; and
    8) check the state of the PM-DEV interface by reading the IPM field of the PM device port SStatus register. If the interface is in partial or slumber state, proceed with this test. If the interface is still active after 10 repetitions of this step, then bypass the rest of this test and put out a message, “Unable to generate DIPM request. PM-08 skipped.”;
c) verify that DIPM requests do not affect other device ports or the PM host port by:
    1) while leaving the HDD in step b connected, connect a second HDD to a different device port. Do not enable DIPM on the second HDD;
    2) initialize both device interfaces;
    3) ensure that the host H-PM interface and both PM-Dev interfaces are active;
    4) enable DIPM in the first HDD and issue a STANDBY IMMEDIATE command to the first drive;
    5) wait 10 s; and
    6) record the states of the H-PM interface and both PM-Dev interfaces;
d) verify PM device port partial/slumber state exit latency;

    NOTE 60 - There is no standard way to cause a device to issue COMWAKE. This test step is a placeholder until a mechanism is defined to allow testing.

    and
e) step d shall be repeated 10 times.

3.20.9.3 Pass/fail criteria

The pass/fail requirements are:

a) verifying that the device supports DIPM is Informative only and not subject to pass/fail evaluation;
b) for each iteration of the test, if the H-PM interface and the second PM-Dev interface are active, and the first PM-Dev interface is in partial or standby state, then the result for this iteration is pass. If either the H-PM interface or the second PM-Dev interface is in partial or slumber state, then the result for this iteration is fail. If all three interfaces are in active state, the result for this iteration is na; and
c) if there is at least one pass result and no fail results, then the test result is pass. If there is one or more fail results, then the test result is fail. If all 10 results are na, then the test result is na.

3.20.10 PM-09 : Speed matching upon resume (H-PM interface)

3.20.10.1 Expected behavior

See Section 8.4.4.3 of Serial ATA Revision 3.5.

The quoted statement below refers to the situation in which a port has received COMWAKE after entering partial or slumber state.

“Calibration and speed negotiation is bypassed since it has already been performed at power-on and system performance depends on quick resume latency. The device, therefore, shall transmit ALIGN$_P$ primitives at the speed determined at power-on.”

In this case, the device refers to the host port of the port multiplier.

3.20.10.2 Measurement requirements

The required measurements are:

1) verify that the H-PM interface running at default speed resumes at the default speed;
2) if the port multiplier supports interface power management using the steps in PM-05, then run the following test:
    1) note the current interface rate – determination of the current interface rate is MOI specific;
    2) issue PMREQ_P or PMREQ_S and confirm that the H-PM interface enters the appropriate low power state;
    3) issue COMWAKE and wait for complete wake of device; and
    4) record the current interface rate – determination of the current interface rate is MOI specific (i.e., it may be obtained by reading the value in the SPD field of the device port SStatus register, or it may be observed directly through a hardware interface monitoring device);

    and
3) repeat the following sequence test 10 times:
    1) verify that the H-PM interface running at reduced speed resumes at the reduced speed;
    2) if the test methodology permits access to the HBA SATA status and control registers and the default rate on the H-PM interface is 3 Gbps, then set the IPM field of the HBA SControl register to limit the interface speed to Gen1 speed. A vendor specific method may be used instead, if available;
    3) issue COMRESET. Confirm that the H-PM interface speed is 1.5 Gbps. If the speed is 3 Gbps, then skip this test step and put out a message, “Unable to force Gen1 speed on Gen2 host to port multiplier interface.”;
    4) if the current speed is 1.5 Gbps, issue PMREQ_P or PMREQ_S and confirm that the interface enters partial or slumber state, as appropriate;
    5) clear the interface speed restriction in the IPM field or vendor specific mechanism and issue COMWAKE; and
    6) confirm that the interface state is active and record the current interface speed.

3.20.10.3 Pass/fail criteria

The pass/fail requirements are:

1) verify that the interface rate does not change before and after the power management sequence. If the interface speed before and after a power management sequence is the same, the result is pass. If the H-PM interface did not enter a low power state when requested or resumed at a different speed, then the result is fail. There is no na result for this test step. If all 10 results are pass, then the test result is pass. If there is a single fail result, then the result for this test is fail; and
2) verify that the H-PM interface running at reduced speed resumes at the reduced speed. If the interface speed before and after a power management sequence is 1.5 Gbps, the result is pass. If the H-PM interface did not enter a low power state when requested or resumed at a different speed, then the result is fail. There is no na result for this test step. If all 10 results are pass, then the test result is pass. If there is a single fail result, then the result for this test is fail.

3.20.11 PM-10 : Speed matching upon resume (PM-Dev interface)

3.20.11.1 Expected behavior

See Section 8.4.4.3 of Serial ATA Revision 3.5.

The quoted statement below refers to the situation in which a port has received COMWAKE after entering partial or slumber state.

“Calibration and speed negotiation is bypassed since it has already been performed at power-on and system performance depends on quick resume latency. The device, therefore, shall transmit ALIGNP primitives at the speed determined at power-on.”

3.20.11.2 Measurement requirements

The required measurements are:

1) check that the port multiplier supports interface power management using the steps in PM-05;
2) attach an HDD supporting HIPM to a device port on the PM;
3) repeat this test 10 times:
    1) initialize the selected device port interface and verify that the interface is active; and
    2) record the current interface speed. Determination of the current interface speed is MOI specific (i.e., it may be obtained by reading the value in the SPD field of the device port SStatus register, or it may be observed directly through a hardware interface monitoring device);
4) repeat this test 10 times:
    1) issue PMREQ_P and confirm that the PM-DEV interface enters partial state;

        NOTE 61 - PMREQ_P is able to be issued on the H-PM interface and be propagated by the PM to the PM-DEV interface, as described in PM-05, or PMREQ_P is able to be issued directly by the PM if the test method has access to the device port registers of the PM.

    2) issue COMWAKE and wait for the PM-Dev interface to become active; and
    3) record the current interface speed;
5) repeat this test 10 times:
    1) issue PMREQ_S and confirm that the PM-DEV interface enters partial state;

        NOTE 62 - PMREQ_S is able to be issued on the H-PM interface and be propagated by the PM to the PM-DEV interface, as described in PM-05, or PMREQ_S is able to be issued directly by the PM if the test methodology permits access to the PM PSCRs.

    2) issue COMWAKE and wait for the PM-Dev interface to become active; and
    3) record the current interface speed;
6) repeat this test 10 times:
    1) verify that the H-PM interface running at reduced speed resumes at the reduced speed;
    2) if the test methodology permits access to the PM PSCRs and the default rate on the PM-Dev interface is 3 Gbps;
    3) set the IPM field of the PM port SControl register to limit the interface speed to Gen1 speed. A vendor specific method may be used instead, if available;
    4) issue COMRESET;
    5) confirm that the PM-Dev interface speed is 1.5 Gbps. If the speed is 3 Gbps, then skip this test step and put out a message, “Unable to force Gen1 speed on Gen2 port multiplier to device interface.”;
    6) if the current speed is 1.5 Gbps, issue PMREQ_P and confirm that the PM-DEV interface enters partial state (see note in equivalent step in step 5, above);
    7) issue COMWAKE and wait for the PM-Dev interface to become active; and
    8) record the current interface speed;
7) repeat this test 10 times:
    1) issue COMRESET. Confirm that the PM-Dev interface speed is 1.5 Gbps. If the speed is 3 Gbps, then skip this test step and put out a message, “Unable to force Gen1 speed on Gen2 port multiplier to device interface.”;
    2) if the current speed is 1.5 Gbps, issue PMREQ_S and confirm that the PM-DEV interface enters slumber state (see note in equivalent step in step 5, above);
    3) issue COMWAKE and wait for the PM-Dev interface to become active; and
    4) record the current interface speed;

    and
8) repeat this test 10 times:

1) clear the interface speed restriction in the IPM field or vendor specific mechanism;
2) issue COMRESET;
3) confirm that the interface state is active; and
4) record the current interface speed.

3.20.11.3 Pass/fail criteria

The pass/fail requirements are:

4) verify that the PM-Dev interface running at default speed resumes at the default speed. If the interface speed before and after each power management sequence (20 total) is the same, the result of the test step is pass. If the PM-Dev interface did not enter a low power state when requested or resumed at a different speed, then the result of the test step is fail. There is no na result for this test step. If all 10 PMREQ_P results are pass, then the PMREQ_P test result is pass. If there is a single fail result, then the result for this test is fail. Put out a message indicating a rate matching failure for PMREQ_P/COMWAKE sequence. If all 10 PMREQ_S results are pass, then the PMREQ_S test result is pass. If there is a single fail result, then the result for this test is fail. Put out a message indicating a rate matching failure for PMREQ_S/COMWAKE sequence; and
5) verify that the H-PM interface running at reduced speed resumes at the reduced speed. If the interface speed before and after each power management sequence is 1.5 Gbps, the result is pass. If the H-PM interface did not enter a low power state when requested or resumed at a different speed, then the result is fail. There is no na result for this test step. If all 10 PMREQ_P results are pass, then the PMREQ_P test result is pass. If there is a single fail result, then the result for this test is fail. Put out a message indicating a rate matching failure for PMREQ_P/COMWAKE sequence. If all 10 PMREQ_S results are pass, then the PMREQ_S test result is pass. If there is a single fail result, then the result for this test is fail. Put out a message indicating a rate matching failure for PMREQ_S/COMWAKE sequence.

3.20.12 PM-11 : Port multiplier reset response

3.20.12.1 Expected behavior

Three types of SATA device reset events are able to be presented by a host to a port multiplier:

a) COMRESET OOB sequence:
   A) from Serial ATA Revision 3.5, Section 13.16.2.2, a host initiated COMRESET has the following effects:
      1) clears any internal state and resets all parts of the Port Multiplier hardware; and
      2) places the reset values in all Port Multiplier registers, including port specific registers. The reset values shall disable all device ports;
   B) the expected behavior following COMRESET is defined by the port multiplier hot plug state machine. See Serial ATA Revision 3.5, Section 13.17. PM behavior follows one of two sequences depending on whether the host sends a FIS to the Control Port (PM-aware host) or does not send a FIS to the Control Port within < 10 ms (non-PM-aware host);
b) Soft Reset from Host to Control Port of PM. The only action taken by a port multiplier that receives a soft reset directed to its control port is to return the unique port multiplier signature FIS, described in Serial ATA Revision 3.5, Section 13.16.2.3; and
c) DEVICE RESET command received from the host by the Control Port of the PM. This ATAPI command is treated as an unsupported command by port multipliers. The PM response shall be a FIS34h with ERR and ABRT bits set to one. See Serial ATA Revision 3.5 Section 16.3.3.8.7.

3.20.12.2 Measurement requirements

The required measurements are:

1) for setup consistency, issue Soft Reset to Port F of the port multiplier before starting the test sequence;
2) with no devices attached, force an interface initialization sequence between the host and the port multiplier host port;
3) check the contents of the mandatory GSCRs and PSCRs to ensure that they are set to their default values (including all device ports disabled);

4) with two devices attached, one to device Port 0 and the other attached to a higher numbered supported port, force an interface initialization sequence between the host and the port multiplier host port;
5) wait 500 ms;
6) verify that the Port 0 SStatus register IPM field shows the link to be Active and the higher numbered port shows the link to be disabled;
7) with at least one device attached to the PM, with its interface in Active state, issue a soft reset to the PM Control Port. A FIS 34h shall be returned. The SATA link on the device port shall remain Active; and
8) issue a DEVICE RESET command to the PM Control Port.

3.20.12.3 Pass/fail criteria

The pass/fail requirements are:
1) all mandatory registers contain their default values;
2) all mandatory PM registers except those for device Port 0 contain their default values;
3) the port multiplier signature FIS has the correct contents;
4) the device port remains in Active state; and
5) the port multiplier returns a FIS 34h with ERROR and ABRT bits set to one.

3.20.13 PM-12 : Device Port 0 hot plug with non-PM aware host software

3.20.13.1 Expected behavior

When host software has no port multiplier support, it shall not send a FIS to the PM Control Port under any circumstances. If device Port 0 receives a COMINIT signal from an attached device, as shall happen if a device is hot plugged, Port 0 shall complete the OOB sequence. The device is required to send a signature FIS34h at that point. If the PM has not detected any FIS transmissions from the host to the Control Port, it assumes legacy mode operation and forwards the signature FIS to the host. From the host perspective, this is identical to a device being hot plugged directly into a host port.

3.20.13.2 Measurement requirements

The required measurements are:
1) with the port multiplier connected to the host system and no devices attached to the port multiplier, apply power to the host system and port multiplier. Do not access Port F of the port multiplier. This should ensure that PM Port 0 is operating in legacy mode; and
2) connect a drive to device Port 0 (drive power may be applied concurrently or beforehand).

3.20.13.3 Pass/fail criteria

Correct signature FIS for an ATA disk drive is received by the host system.

3.20.14 PM-13 : Hot plug with PM aware host software

3.20.14.1 Reference

See Section 16.3.3.5 and 16.3.3.10 of Serial ATA Revision 3.5.

3.20.14.2 Expected behavior

All device ports except 0 operate only with PM-aware host software. If the host system sends a FIS to the port multiplier Control Port before device Port 0 completes a COMRESET sequence, then device Port 0 operates in this mode as well. The significant difference for test purposes is that a device port in “PM-aware” mode shall not have a signature FIS propagated to the host system after a COMRESET sequence. Instead, the X bit in the SError register of the affected port shall be set to one.

By default, if any installed device port has its X bit set to one, a bit shall be set in GSCR[32] indicating that condition. There is one bit per port and a mask selecting which bits in the device port SError registers shall turn on the GSCR[32] bit for that port.

The X bit in a device port SError register shall only be set to one when the port is Active. Hot plugging a device into a port that has been and remains Disabled does not result in the X-bit for that port being set.

3.20.14.3 Measurement requirements

The required measurements are:

1) for setup consistency, issue Soft Reset to Port F of the port multiplier before starting the test sequence;
2) with the port multiplier connected to the host system and no devices attached to the port multiplier, apply power to the host system and port multiplier;
3) reset all bits to zero in the SError registers of device Port 0 and a selected device port numbered > 0;
4) reset all bits to zero in GSCR[32];
5) connect a drive to device Port 0 (drive power may be applied concurrently or beforehand) to the selected device port numbered > 0;
6) initialize the interfaces on these ports to the Active state;
7) reset all bits to zero in the SError registers of device Port 0 and a selected device port numbered > 0;
8) reset all bits to zero in GSCR[32];
9) disable the SATA interface on these 2 ports by writing 0100b to the DET field of the respective SControl registers; and
10) connect a drive to device Port 0 (drive power may be applied concurrently or beforehand) to the selected device port numbered > 0. Do not initialize the interfaces of these two ports.

3.20.14.4 Pass/fail criteria

The pass/fail requirements are:

1) read the SError register for device Port 0 and verify that bit 26 is set to one (this is the X bit for device Port 0);
2) for the selected device port numbered >0, check that the corresponding bit number in GSCR[32] is set to one (e.g., if the selected device Port is 5, then check bit 5);
3) verify that bit 26 in the SError register for the device port being tested is set to one; and
4) for test step 2, above, verify that the X-bit is cleared in the SError registers of both device ports and that the GSCR[32] bits corresponding to the two ports is cleared to zero.

3.20.15 PM-14 : FIS sent to a disabled device port

3.20.15.1 Reference

See Section 16.3.3.8.3 of Serial ATA Revision 3.5.

3.20.15.2 Expected behavior

When a port multiplier receives a FIS from the host system directed to a device port that is disabled, it shall not respond with either R_OK or R_ERR. Instead, it shall send a SYNC primitive to the host system, terminating the FIS transfer.

There is no standard way for host software to know that the HBA has received SYNC from the PM. The expected result shall be a command timeout in host software.

3.20.15.3 Measurement requirements

The required measurements are:

1) for setup consistency, issue Soft Reset to Port F of the port multiplier before starting the test sequence;
2) install a SATA analyzer on the link between HBA and port multiplier;
3) install a drive on one of the device ports and initialize the interface;
4) verify that the drive is able to run an IDENTIFY DEVICE command correctly;

NOTE 63 - In addition to performing the tests below through a host system with a SATA HBA, the tests may also be performed by using a SATA emulator/analyzer in place of the host system and HBA.

5) disable the interface to the attached drive by writing 0100b to the DET field of the SControl register of the port where the drive is attached;
6) issue an IDENTIFY DEVICE command to the attached device;
7) observe whether the command completes successfully;
8) capture a trace of the interface activity when the command is issued;
9) enable the device port to which the test drive is attached;
10) verify that the drive can run an IDENTIFY DEVICE command correctly;
11) unplug and replug drive power (simulated hot plug). This should set to one the X bit for this device port and block FIS transfers to and from the port until the X bit is cleared to zero;
12) issue an IDENTIFY DEVICE command to the attached device;
13) observe whether the command completes successfully after the simulated hot plug; and
14) capture a trace of the interface activity when the command is issued.

3.20.15.4 Pass/fail criteria

The pass/fail requirements are:

1) verify that the command did not complete successfully by examining the interface trace from the analyzer that the PM responded to the command FIS with one or more SYNC primitives;
2) verify that the command after the simulated hot plug did not complete successfully by examining the interface trace from the analyzer that the PM responded to the command FIS with one or more SYNC primitives; and
3) read the SError register of the device port and verify that the X bit, bit 26 is set to one.

3.20.16 PM-15 : FIS sent to an invalid device port address

3.20.16.1 Reference

See Section 16.3.3.8.4 of Serial ATA Revision 3.5.

3.20.16.2 Expected behavior

When a port multiplier receives a FIS from the host system directed to a device port that is beyond the range of supported port numbers, it shall not respond with either R_OK or R_ERR. Instead, it shall send a SYNC primitive to the host system, terminating the FIS transfer.

This test does not apply to a port multiplier that supports the full range of allowable device port numbers, 0 to 14.

There is no standard way for host software to know that the HBA has received SYNC from the PM. The usual result may be a command timeout in host software.

3.20.16.3 Measurement requirements

The required measurements are:

1) for setup consistency, issue Soft Reset to Port F of the port multiplier before starting the test sequence;
2) install a SATA analyzer on the link between HBA and port multiplier. Install a drive on the highest numbered device port and initialize the interface. Verify that the drive is able to run an IDENTIFY DEVICE command correctly; and
3) issue an IDENTIFY DEVICE command to a port address greater than the highest numbered port on the PM. Observe whether the command completes successfully. Capture a trace of the interface activity when the command is issued.

3.20.16.4 Pass/fail criteria

The pass/fail requirements are:

a) verify that the command did not complete successfully; and

b) verify by examining the interface trace from the analyzer that the PM responded to the command FIS with one or more SYNC primitives.

3.20.17 PM-16 : Test for PM-aware host

3.20.17.1 Reference

See Section 13.16.3.2 of Serial ATA Revision 3.5.

3.20.17.2 Overview

Port Multiplier aware software checks the host's SStatus register to determine if a device is connected to the port. If a device is connected to the port, then the host issues a software reset to the control port. If the Port Multiplier signature is returned, then a Port Multiplier is attached to the port. Then the host proceeds with enumeration of devices on Port Multiplier ports as detailed in Section 13.16.4.2 of Serial ATA Revision 3.5.

3.20.17.3 Expected behavior

Following system power on, a PM-aware host shall issue Soft Reset to port FFh, and wait for the specific signature FIS of a port multiplier. This is in contrast to a non-PM-aware host, which is not aware of PM port address 0F and which waits for a signature FIS from a direct attached device.

After determining that a port multiplier is attached, the PM-aware host shall enumerate the PM ports and discover any attached devices. The exact sequence of events on the host port after the PM signature FIS is implementation specific and is not detailed here.

3.20.17.4 Measurement requirements

The required measurements are:

1) with a SATA analyzer connected between the designated HBA port and the PM host port, program the analyzer to capture all FIS transfers;
2) start the analyzer;
3) power up the host system and the port multiplier. If the port multiplier is powered by a separate power supply, then power up the port multiplier before turning on the host system being tested; and
4) after the host OS is fully loaded and initialized, stop the analyzer.

3.20.17.5 Pass/fail criteria

The pass/fail requirements are:

a) in order for the host to be designated PM-aware, the trace is required to show a soft reset addresses to the control port of the port multiplier;
b) a soft reset consists of two consecutive Register Host -> Device FISes sent by the host. The first shall have the C bit cleared to zero and Control register bit 2 set to one. The second shall have the C bit = 0 and Control register bit 2 cleared to zero. In both FISes the PM Port field shall = FFh; and
c) if the port multiplier is working properly, it shall send a Register Device -> Host FIS containing the port multiplier signature as defined in Serial ATA Revision 3.5, Section 16.3.3.11.2, Figure 254 after the soft reset completes.

4 System interoperability tests

4.1 Overview

The system interoperability tests are required tests above and beyond the tests described in the preceding sections of the document. This testing is required for the Device and Host product types. No System Interoperability testing is required for Cable products.

4.2 System description

The test systems used for the system interoperability testing shall be configured in such a way to confidently provide test capabilities to ensure interoperability of a Serial ATA product within that platform. The products and configuration information for the test platforms are defined in the following sections.

4.2.1 System product selection

Five different system configurations shall be defined for use when testing for system interoperability. These systems shall preferably be products that are commercially available and are recognized on the Integrators list. It is required that all 5 configurations are used in verification of all SATA products under test (PUT), (i.e., hosts and devices), and that the PUT pass the System Interop test in all 5 different system configurations to be eligible for the SATA-IO Integrators List.

The SATA-IO Integrator's List serves as the approved list for test products for use at Interop Workshops and independent test labs. For the Interoperability Program, a system is defined as having the following components:

a) host;
b) device; and
c) cable (not applicable for direct attached systems, e.g., mobile).

Only one PUT shall be tested in a system at a time. The host/device that a PUT is tested in within the System Interoperability tests is referred to as the Test Bed Product.

Test Providers (whether they are SATA-IO Gold Suite providers or approved Test Labs) shall maintain a public list of Test Bed Products available for interop testing at their facility. Test Bed Products shall be available at the test facility for at least 18 months in order to allow for necessary tests to be reproduced.

The following sections define the non-PUT component requirements.

4.2.2 System interoperability non-PUT cable requirements

For all system interoperability tests, any SATA cable available may be used to connect the PUT to the Test Bed Product. Test providers are responsible for ensuring that the cables used are in good condition. The cables may be internal or external SATA cables. An external SATA cable may be used in conjunction with any available eSATA bracket as a means to connect the PUT and the Test Bed Product.

4.2.3 System interoperability host requirements for device testing

The Test Bed Host may be any complete PC system or motherboard with a SATA or eSATA interface from the Integrator's List.

When a PUT is listed on the SATA-IO Integrators List, the SATA features supported by the PUT shall also be listed.

The following platform configurations shall be used for all Gen1 or Gen2 system interoperability device product testing. Of the 5 Test Bed Hosts used for System Interop testing, at least 3 different SATA Phy Interfaces shall be represented (different IP providers):

a) configuration 1 - any Host System operating at Gen1, Gen2, or Gen3 speeds. The Host system used shall transmit with SSC on;
b) configuration 2 - any Host System operating at Gen1, Gen2, or Gen3 speeds;
c) configuration 3 - any Host System operating at Gen1, Gen2, or Gen3 speeds;
d) configuration 4 - any Host System operating at Gen1, Gen2, or Gen3 speeds; and
e) configuration 5 - any Host System operating at Gen1, Gen2, or Gen3 speeds.

The following platform configurations shall be used for all Gen3 system interoperability device testing. Of the 5 Test Bed Hosts used for System Interop testing, at least 3 different SATA Phy Interfaces shall be represented (different IP providers):

a) configuration 1 - any Host System operating at Gen3 speeds. The Host system used shall transmit with SSC on;
b) configuration 2 - any Host System operating at Gen3 speeds;
c) configuration 3 - any Host System operating at Gen1, Gen2, or Gen3 speeds;
d) configuration 4 - any Host System operating at Gen1 or Gen2 speeds; and
e) configuration 5 - any Host System operating at Gen1 or Gen2 speeds.

4.2.4 System interoperability device requirements for host testing

In order to use a SATA or eSATA Device as a Test Bed Product for the purpose of System Interoperability testing for a host, a Test Provider must choose devices from the SATA-IO Integrators List.

The following platform configurations shall be used for all Gen1 or Gen2 system interoperability device product testing. Of the 5 Test Bed Devices used for System Interop testing, at least 3 different SATA Phy Interfaces shall be represented (different IP providers):

a) configuration 1 - any Device operating at Gen1, Gen2, or Gen3 speeds. The Device used shall transmit with SSC on;
b) configuration 2 - any Device operating at Gen1, Gen2, or Gen3 speeds;
c) configuration 3 - any Device operating at Gen1, Gen2, or Gen3 speeds;
d) configuration 4 - any ODD Device operating at Gen1 speed. The Device used shall transmit with SSC on; and
e) configuration 5 - any ODD Device operating at Gen1 speed.

The following platform configurations shall be used for all Gen3 Host system interoperability product testing. Of the 5 Test Bed Devices used for System Interop testing, at least 3 different SATA Phy Interfaces shall be represented (different IP providers):

a) configuration 1 - any Device operating at Gen3 speed. The Device used shall transmit with SSC on;
b) configuration 2 - any Device operating at Gen3 speed;
c) configuration 3 - any Device operating at Gen2 speed;
d) configuration 4 - any ODD Device operating at Gen1 speed. The Device used shall transmit with SSC on; and
e) configuration 5 - any ODD Device operating at Gen1 speed.

If a host PUT does not support a device product type:

a) the non-supported device type shall be indicated on the Product Info sheet. Failure to indicate non-support with a failure on a non-supported device still results in a System Interop failure;
b) additional devices from the support device types shall be substituted for the non-support product type to maintain the required number of configurations; and
c) non-supported device types shall be indicated if the product is added to the Integrators List.

4.3 System interoperability test description

4.3.1 Overview

There are several key concerns when working to understand the interoperability of a product in a specified system, including data transfer and error rates. The system interoperability tests are defined in a way such that the products are validated in a repeatable and consistent manner.

4.3.2 Resource requirements

The following tools shall be needed to validate the System Interoperability test tool:

a) SATA bus analyzer capable of acquiring traces for all supported product types and capturing both data level and command level traces; and
b) SATA bus error injector capable of causing a data corruption error in a DATA FIS.

4.3.3 SYS-01: System interoperability test requirements

4.3.3.1 Data pattern

The data pattern used by System Interoperability test shall use the long version of the Composite Pattern payload defined by 7.4.5.4.7 of Serial ATA Revision 3.5. The host typically scrambles and encodes the data before it is transmitted on the SATA interface. The source data pattern shall be designed to take this into consideration such that the proper payload pattern is still presented on the SATA interface.

4.3.3.2 FIS alignment and size

The System Interoperability test shall present (for writes) or request (for reads) the first byte of each data pattern be the first byte of a data FIS. Subsequent data FIS alignment is highly suggested but not required. Usage of 8 kB data FISs is highly suggested but not required. The reason is the Long COMP data pattern is 8 kB and 8 kB FIS usage keeps the designed pre-disparity pre-scrambling intact.

4.3.3.3 SError and SStatus host registers

The System Interoperability test should monitor, if possible, the host SError and SStatus registers:

a) SError - if any bit in the SError register (Bit W shall be excluded), it shall be counted as an error and cleared; and
b) SStatus - any change to the SStatus SPD bits shall be counted as an error.

4.3.3.4 Data Pattern sizes

The data pattern shall use all of the following pattern sizes in the prescribed combination. The 8 KiB (Kibi Bytes) data pattern is one complete Long COMP data pattern as defined above. Each additional pattern size is defined as exact repeating multiples of the 8 KiB data pattern. Each size represents a binary value *not* a decimal value (i.e., 8 KiB = 8 × 1 024 = 8 192 Bytes, 1 MiB = 1 × 1 024 × 1 024 = 1 048 576 Bytes):

a) 8 KiB;
b) 64 KiB;
c) 256 KiB;
d) 1 MiB; and
e) 16 MiB.

The purpose of using multiple size files is to strike a balance between guaranteed being 8 KiB FIS aligned and increased data throughput that is gained with larger file sizes. In addition, the smaller file sizes have a high likelihood of being cached on many products, and thus achieving higher burst transfer rates, whereas the larger files increase the devices media access interactions.

4.3.3.5 Host caching and retries

The System Interoperability test shall be configured such that:

a) no host caching of data is performed. All transfer requests shall be presented on the SATA interface;
b) the host is only allowed to retry non-data FISs without notification to the test tool; and
c) the host shall *not* retry data without notification to the test tool.

4.3.3.6 Data file signatures

Each data file shall have a stored industry standard 128-bit MD5 signature that shall be used for data validity verification. The test tool shall use MD5 signatures supplied by the SATA-IO.

4.3.3.7 HDD data pattern set

For a HDD PUT a single data pattern set is defined as follows:

1) 8 KiB file, 40 generational copies, last file signature verified;

2) 64 KiB file, 40 generational copies, last file signature verified;
3) 256 KiB file, 40 generational copies, last file signature verified;
4) 1 MiB file, 40 generational copies, last file signature verified; and
5) 16 MiB file, 40 generational copies, last file signature verified.

A generational copy is defined as follows:

1) first read of the copy, comes from the original data source, not the PUT;
2) the first write, using the data from the first read is written to the PUT;
3) the second read comes from the first write data on the PUT;
4) the second write comes from the second read, but writes to a second file location on the PUT;
5) ….;
6) the thirty ninth read comes from the thirty eighth write data on the PUT;
7) the fortieth write comes from the thirty ninth read on the PUT, but writes to the fortieth file location on the PUT; and
8) the fortieth read comes from reading the file on the PUT to generate the MD5 signature for comparison.

4.3.3.8 ATAPI data pattern set

For an ATAPI PUT a single data pattern set is defined as follows:

1) 8 KiB file, read and signature verified 40 times;
2) 64 KiB file, read and signature verified 40 times;
3) 256 KiB file, read and signature verified 40 times;
4) 1 MiB file, read and signature verified 40 times; and
5) 16 MiB file, read and signature verified 40 times.

4.3.3.9 Test duration

The System Interoperability test shall repeat the data pattern set until a minimum of 9 min of execution time has been reached for each of the required configurations with error checking continuously enabled.

4.3.3.10 Stop on error

The System Interoperability test may stop on first error or count/indicate error and continue to complete the test duration.

4.3.4 System interop pass/fail criteria

The pass/fail requirements are:

a) the test tool shall count and report each data error (retried or not);
b) one or more data errors fails that that configuration and no time or transfer size shall be reported; and
c) a product under test shall pass a minimum of 4 of the 5 configurations.

Table 22 – System Interop Test Name matrix

	Loops or errors	# MiB (1 024 × 1 024 bytes)	Time (s)
Config 1	SYS-01a	SYS-01b	SYS-01c
Config 2	SYS-01a	SYS-01b	SYS-01c
Config 3	SYS-01a	SYS-01b	SYS-01c
Config 4	SYS-01a	SYS-01b	SYS-01c
Config 5	SYS-01a	SYS-01b	SYS-01c

4.4 System interoperability test tool validation requirements

4.4.1 Overview

A certified System Interoperability test tool shall be validated on all applicable hosts (maximum of 3 different hosts is required, more is allowed), using a minimum of 3 device products from each supported device type.

See Section 4.3.3.7 for data pattern size definitions.

4.4.2 SYT-01 – Data pattern validation

4.4.2.1 Device expected behavior

The test tool shall present the 8 KiB Long COMP data pattern on the SATA interface.

4.4.2.2 Measurement requirements

While reading a single 8 KiB Long COMP data pattern file:

1) with a SATA bus analyzer, validate Long COMP data pattern is correct and complete; and
2) generate an MD5 checksum while the data file is being read.

4.4.2.3 Pass/fail criteria

Pass if all of the following are true, then pass, otherwise fail:

1) the 8 KiB Long COMP data pattern is verified to be correct and complete; and
2) the MD5 signature shall match the SATA-IO Logo published MD5 signature.

4.4.3 SYT-02 – Data pattern alignment

4.4.3.1 Device expected behavior

The test tool shall present the first Dword of the Long COMP data pattern as the first Dword of a DATA FIS on the SATA interface.

4.4.3.2 Measurement requirements

Using the 8 KiB Long COMP data pattern, with a SATA bus analyzer, with complete data capture, validate the first Dword of the Long COMP data pattern is the first Dword of a DATA FIS on the SATA interface for a minimum of 3 consecutive data patterns.

4.4.3.3 Pass/fail criteria

If the first Dword of the DATA FIS matches and aligns with the first Dword of the 8 KiB Long COMP data pattern, then pass, otherwise fail.

4.4.4 SYT-03 – 8 KiB data FIS usage

4.4.4.1 Device expected behavior

The test tool shall present the 8 KiB data pattern as a single 8 KiB DATA FIS on the SATA interface. Only applicable if test tool supports HDD Device type.

4.4.4.2 Measurement requirements

Using the 8 KiB data pattern on a HDD, with a SATA bus analyzer, validate the 8 KiB data pattern is completely contained in an 8 KiB DATA FIS on the SATA interface a minimum of 3 consecutive data patterns.

4.4.4.3 Pass/fail criteria

If for 3 consecutive DATA FIS both of the following are true, then pass, otherwise fail:

a) each data FIS contains exactly 8 KiB of data; and
b) each data FIS matches the Long COMP data pattern.

4.4.5 SYT-04 – Data error detection

4.4.5.1 Device expected behavior

The test tool shall detect any SATA DATA error.

4.4.5.2 Measurement requirements

Using an error injection tool, change the data in the data FIS to cause a CRC error in the DATA FIS.

4.4.5.3 Pass/fail criteria

The test tool shall detect, report, and indicate failure upon the receipt of a single error even if the transfer is retried.

4.4.6 SYT-05 – Complete data set, including host caching and retries

4.4.6.1 Device expected behavior

The test tool shall demonstrate a complete (no missing or additional data) and proper data set is transferred, including no host caching is being performed.

4.4.6.2 Measurement requirements

With a bus analyzer, demonstrate that a complete (no missing or additional) data pattern set for each device type is transferred on the SATA bus for each test tool request. Traces that filter the user data but still indicate the FIS structure are acceptable. Reads of non-data set (file system reads) are allowed but should be minimized.

4.4.6.3 Pass/fail criteria

The pass/fail requirements are:

a) a complete data pattern set for each device type is transferred on the SATA bus for each test tool request; and
b) any additional data files shall indicate a fail (i.e., reading the data for the copy and reading the same data for signature generation is a tool failure).

4.4.7 SYT-06 - Data file signatures

4.4.7.1 Measurement requirements

The test tool shall provide documentation (signature file or code snippet with MD5 signatures) showing only the SATA-IO Logo MD5 data file signatures are used for data integrity validation.

4.4.7.2 Pass/fail criteria

All MD5 signatures used shall match the SATA-IO Logo MD5 signatures.

4.4.8 SYT-07 - Data pattern set

4.4.8.1 Measurement requirements

The test tool shall provide documentation showing the proper data pattern set is used for all supported device types.

4.4.8.2 Pass/fail criteria

Provide log files or test code showing the proper data pattern set is used for each supported device type.

4.4.9 SYT-08 - Test duration

4.4.9.1 Measurement requirements

The test tool shall demonstrate on one supported device type and provide documentation for all other supported device types showing the tests processed for a minimum of 9 min for all supported device types.

4.4.9.2 Pass/fail criteria

For each of the supported device types, provide time stamped log files (with embedded starting and end times) showing a minimum of 9 min execution time.

4.4.10 SYT-09 – System configuration

4.4.10.1 Measurement requirements

The test tool is required to support all possible system configurations and only the test tool generated traffic shall be sent/received to/from the PUT.

The OS shall not access the PUT once the test has begun (i.e., the swap file shall not be on the PUT).

Test tool code may be located on the PUT as long as it is completely loaded from the PUT before the test is started and all accesses to the PUT are the previously defined System Interop FCOMP pattern until the test is complete.

All log files shall be written to a non-PUT media or stored in RAM until all tests are complete.

4.4.10.2 Pass/fail criteria

Command level bus traces showing only Framed COMP pattern transfers for the complete test period.

4.4.11 SYT-10 – OS install

4.4.11.1 Measurement requirements

All test tool validation shall be performed after the OS has been installed. If the OS is installed on the PUT, then the validation shall be done on every PUT (i.e., the OS and driver combination used during test tool validation shall be the same as that used during the PUT validation). If any OS or driver updates are made, the test tool is required to be re-validated. No OS or driver updates are allowed between tool validation and PUT validation.

4.4.11.2 Pass/fail criteria

Directory of PUT showing no operating system files or Logs from test tool validation and the PUT validation showing the OS/drivers are identical (MD5 signatures of critical files are one such way).

5 Calibration and verification of jitter measurement devices (JTF Cal)

5.1 Purpose

To calibrate and verify the JMD and associated test setup has a proper response to jitter and SSC. Currently these JTF considerations are only for the following interfaces, Gen1i, Gen1m, Gen2i, Gen2m, and Gen3i.

5.2 References

Serial ATA Revision 3.5 Gold.

5.3 Resource requirements

Resources required for calibration:

a) Pattern Generator for SATA signals;
b) Sine wave source, 30 kHz, and 0.5 MHz to 50 MHz;
c) Test cables; and
d) Jitter Measuring Device.

5.4 Discussion

The response to known jitter levels of a JMD is calibrated and verified in two frequency bands. The lower frequency band is to verify proper JTF suppression of the phase jitter created by SSC (30 kHz) and the second higher frequency band is in the transition region between the reference clock tracking and not tracking the jitter (e.g., 2.1 MHz for Gen1 and Gen2, 4.2 MHz for Gen3). The reference clock is part of the JMD and may be implemented in hardware or software. By calibrating the JMD to these two bands, the response to jitter is calibrated to the SATA Gen1, Gen2, or Gen3 jitter definitions and allows for improved correlation among JMDs.

For Gen1 and Gen2, the lower frequency band requirement is tested with a D24.3 pattern on which 20.8 ns with a relative tolerance of ± 10 % sinusoidal phase (time) modulation at 30 kHz is added. The ratio of the reported jitter to the amount actually applied (measured independently) is the attenuation and shall meet the −72 dB ± 3 dB requirement.

For Gen3, the lower frequency band requirement is tested with a D24.3 pattern on which 1.0 ns with a relative tolerance of ± 10 % sinusoidal phase (time) modulation at 420 kHz is added. The ratio of the reported jitter to the amount actually applied (measured independently) is the attenuation and shall meet the -38.2 dB ± 3 dB requirement.

This test is related to the Serial ATA Revision 3.5. The Specification defines two parameters related to SSC, f_{baud} the baud rate respectively 1.5 Gbps for Gen1, 3 Gbps for Gen2, or 6 Gbps for Gen3 and SSC_{tol} the spread spectrum modulation deviation. The frequency deviation (of the clock in the data source) is related to the spread spectrum modulation (SSC) frequency deviation by

$$\Delta f = SSC_{tol} \ f_{baud}$$

The sinusoidal phase modulation is related to frequency modulation by

$$\Delta f = f_m \ \Delta\phi$$

where:

Δf is the frequency deviation in Hz;

f_m is the modulation frequency in Hz; and

$\Delta\phi$ is the phase deviation in radians.

The phase deviation is related to the phase modulation in time by

$$\Delta\phi = 2\pi \ f_{baud} \ \Delta T$$

From these relationships, an expression for the SSC frequency deviation from the JTF test parameters is given, calculated for the test conditions and shown to be within the Specification limits.

$$SSC_{tol} = 2\pi \ f_m \ \Delta T = 2\pi \left(30 \times 10^3\right)\left(20.83 \times 10^{-9}\right) = 3\,926\,ppm$$

From these calculations, either frequency or phase modulation may be used. A separate means of verifying the level of the modulation is used to make sure the test conditions are correct. The independent separate means of verification of the 30 kHz test signal is equivalent to a frequency demodulator or wide range phase demodulator. Realizations of this are:

a) time interval error plot with constant frequency clock on a real time oscilloscope;
b) equivalent time oscilloscope; and
c) frequency demodulator.

Two tests are performed in the upper frequency band, the adjustment of the -3 dB BW of the JTF (2.1 MHz for Gen1 and Gen2, 4.2 MHz for Gen3) and the verification of the peaking (3.5 dB maximum). Both of these tests use a D24.3 pattern with sinusoidal periodic phase modulation, or periodic jitter (PJ) that has been independently verified to produce a peak-to-beak amplitude of 0.3UI with a relative tolerance of ± 10 % (200 ps for Gen1, 100 ps for Gen2, or 50 ps for Gen3) consistently over a frequency range of 0.5 MHz to 50 MHz. In both tests a 0 dB reference level is initially determined as the measured PJ phase jitter amplitude at 50 MHz and all other attenuation magnitude measurements are normalized to this level, not the absolute level of the source. It is important that the PJ source level does not vary in amplitude over this test range, or the variation shall be extracted in the final calculations.

For the tests in the upper frequency band shall have a phase or jitter modulator. The independent separate means of verification of the 2.1 MHz, 4.2 MHz, and 50 MHz test signals is equivalent to a deterministic jitter measurement with constant clock. Realizations of this are time interval error plot with constant frequency clock on a real time oscilloscope, equivalent time oscilloscope with histogram and constant frequency clock, bit error rate tester (BERT) and constant frequency clock, and spectral analysis.

There are two typical JMD adjustments for clock recovery, “loop BW” and another known as “peaking” or “damping” or ζ. These adjustments may refer to the closed loop response or be specific to a particular design, so they shall be used directly to ensure the JTF response to jitter. It is suggested that the “loop BW” be adjusted initially (with the “peaking” fixed) and if both the low frequency band requirements and the high frequency band requirements shall both be simultaneously be met, the “peaking” be adjusted to modify the JTF shape in the upper band. In the case of hardware based reference clocks, moderate levels of “peaking” may be required to achieve the proper attenuation at 30 kHz or 420 kHz. The “peaking” setting is usually specific to the JMD. With software based clock recovery, the suggested starting “peaking” level or “damping” may be low, close to the critically damped condition of ζ = 0.707.

The test sequence for all measurements also removes the baseline deterministic jitter, DJ of the source and JMD such that what is being measured is the reported jitter only due to the added test jitter and not any baseline residual jitter in the test system. This is important to insure the accuracy of the measurement at low reported jitter levels.

5.5 Test procedure

The response to jitter of the JMD (the reference clock is part of the JMD) is measured with three different jitter modulation frequencies corresponding to the three cases:

a) SSC (full tracking);
b) jitter (no tracking); and
c) the boundary between SSC and jitter.

The jitter source is independently verified by separate means. This ensures the jitter response of the JMD is reproducible across different test setups.

The three Gen1 test signals are:

a) a 375 MHz square wave with a relative tolerance of ± 0.035 % (which is a D24.3, 0011 0011b pattern) with rise time between 67 ps and 136 ps (20 % to 80 %) [1] with a sinusoidal phase modulation with a peak-to-peak amplitude of 20.8 ns with a relative tolerance of ± 10 % at 30 kHz with a relative tolerance of ± 1 %;
b) a 375 MHz square wave with a sinusoidal phase modulation with a peak-to-peak amplitude of 200 ps with a relative tolerance of ± 10 % at 50 MHz with a relative tolerance of ± 1 %; and
c) a 375 MHz square wave with no modulation.

The three Gen2 test signals are:

a) a 750 MHz square wave with a relative tolerance of ± 0.035 % (which is a D24.3, 0011 0011b pattern) with rise time between 67 ps and 136 ps (20 % to 80 %) [1] with a sinusoidal phase modulation with a peak-to-peak amplitude of 20.8 ns with a relative tolerance of ± 10 % at 30 kHz with a relative tolerance of ± 1 %;

b) a 750 MHz square wave with a sinusoidal phase modulation with a peak-to-peak amplitude of 100 ps with a relative tolerance of ± 10 % at 50 MHz with a relative tolerance of ± 1 %; and
c) a 750 MHz square wave with no modulation.

The three Gen3i test signals are:

a) a 1 500 MHz square wave with a relative tolerance of ± 0.035 % (which is a D24.3, 0011 0011b pattern) with rise time between 33 ps and 67 ps (20 % to 80 %) [1] with a sinusoidal phase modulation with a peak-to-peak amplitude of 1.0 ns with a relative tolerance of ± 10 %;
b) a 1 500 MHz square wave with a sinusoidal phase modulation with a peak-to-peak amplitude of 50 ps with a relative tolerance of ± 10 % at 50 MHz with a relative tolerance of ± 1 %; and
c) a 1 500 MHz square wave with no modulation.

An independent separate means of verification of the test signals is used to make sure the level of the modulation is correct.

The test procedure checks two conditions, the JTF attenuation and the JTF bandwidth. Care is taken to minimize the number of absolute measurements taken, making most relative, this reduces the dependencies and improves accuracy.

The test procedure is:

1) for Gen 1 and Gen 2 calibration, adjust the pattern generator for a D24.3 pattern (0011 0011b, with a rise time within specified limits) modulation to produce a 30 kHz with a relative tolerance of ± 1 %, sinusoidal peak-to-peak phase modulation of 20.8 ns with a relative tolerance of ± 10 %. For Gen3 calibration, adjust the pattern generator for a D24.3 pattern (0011 0011, with a rise time within specified limits) modulation to produce a 420 kHz ± 1 %, sinusoidal peak-to-peak phase modulation of 1.0 ns with a relative tolerance of ± 10 %;
2) verify the level of modulation meets the requirements and record the pp level, **DJSSC**. This is done with a Time Interval Error (TIE) type measurement or equivalent;
3) apply test signal to the JMD. Turn off the sinusoidal phase modulation. Record the reported DJ, **DJSSCOFF**;
4) turn on the sinusoidal phase modulation. Record the reported DJ, **DJSSCON**; and
5) calculate and record the level of measured DJ by subtracting the DJ with modulation off from DJ with modulation on, **DJMSSC** = **DJSSCON** - **DJSSCOFF**. Calculate the jitter attenuation by $20Log_{10}$(**DJMSSC** / **DJSSC**). This value shall fall within the range of –72 dB ± 3 dB. Adjust the JMD settings to match this requirement:
    1) adjust the pattern generator for a D24.3 pattern (0011 0011b) and modulation to produce a 50 MHz with a relative tolerance of ± 1 %, sinusoidal peak-to-peak phase modulation of 0.3 UI with a relative tolerance of ± 10 % (i.e., 200 ps for Gen1, 100 ps for Gen2, or 50 ps for Gen3i), also the COMP pattern. (SOF/HEADER/CRC/EOF);
    2) contains leading X_RDY and trailing WTRM/SYNC/CONT primitives to maintain framing protocol consistency;
    3) maintains running disparity (i.e., pattern begins and ends with the same running disparity, so that when it is transmitted continuously, the Monitoring Tool does not detect the leading SOF as a Running Disparity error);
    4) maintains desired $ALIGN_P$ count and spacing (first 2 Dwords are $ALIGN_P$ out of every group of 256 Dwords);
    5) maintains $ALIGN_P$ spacing upon wrapping (requires total pattern length to be an even multiple of 40 × 256 = 10 240 bits. 92 160 = 9 × 10 240); and
    6) overall pattern length is even multiple of 128 bits, 256 bits, and 512 bits, for broad compatibility with known pattern generators.

NOTE 64 - This pattern has been specifically designed for SATA-IO test purposes.

Any deletion/insertion of any symbol(s) other than align primitives or other modification to the exact bit sequence shall render the pattern invalid for the purposes of SATA-IO RSG testing.

NOTE 65 - The raw bit pattern is provided in an external .txt file, which may be downloaded from the SATA-IO website.

5.6 SATA 3.0 ECN 009 long FRAMED COMP pattern

```
   1: +K28.5- BC 1100000101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D27.3+ 7B 1101100011  ALIGN
                                    (Repeat previous Dword until)
   3: +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101
                                    (Repeat previous Dword until)
  10: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D23.2+ 57 1110100101  +D23.2- 57 0001010101  X_RDY
  11: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D23.2- 57 0001010101  -D23.2+ 57 1110100101  X_RDY
  12: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D23.2+ 57 1110100101  +D23.2- 57 0001010101  X_RDY
  13: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D23.2- 57 0001010101  -D23.2+ 57 1110100101  X_RDY
  14: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D23.2+ 57 1110100101  +D23.2- 57 0001010101  X_RDY
  15: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D23.1- 37 0001011001  -D23.1+ 37 1110101001  SOF
  16: +D11.6+ CB 1101000110  +D22.3+ 76 0110100011  +D18.6+ D2 0100110110  + D3.0- C2 0100100110
  17: -D31.3+ 7F 1010110011  +D31.3- 7F 0101001100  -D31.3+ 7F 1010110011  +D31.3- 7F 0101001100
                                    (Repeat previous Dword until)
 257: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
 259: -D31.3+ 7F 1010110011  +D31.3- 7F 0101001100  -D31.3+ 7F 1010110011  +D31.3- 7F 0101001100
                                    (Repeat previous Dword until)
 275: -D21.5- B5 1010101010  -D21.5- B5 1010101010  -D21.5- B5 1010101010  -D21.5- B5 1010101010
                                    (Repeat previous Dword until)
 339: -D24.3+ 78 1100110011  +D24.3- 78 0011001100  -D24.3+ 78 1100110011  +D24.3- 78 0011001100
                                    (Repeat previous Dword until)
 403: -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101
                                    (Repeat previous Dword until)
 467: -D25.6- D9 1001100110  - D6.1- 26 0110011001  -D25.6- D9 1001100110  - D6.1- 26 0110011001
                                    (Repeat previous Dword until)
 513: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
 515: -D25.6- D9 1001100110  - D6.1- 26 0110011001  -D25.6- D9 1001100110  - D6.1- 26 0110011001
                                    (Repeat previous Dword until)
 533: -D17.7+ F1 1000110111  +D30.7+ FE 1000011110  + D7.1+ 27 0001111001  +D14.7- EE 0111001000
 534: -D30.7- FE 0111100001  - D7.6- C7 1110000110  -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100
 535: -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100  -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100
                                    (Repeat previous Dword until)
 769: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
 771: -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100  -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100
                                    (Repeat previous Dword until)
1025: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
1027: -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100  -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100
                                    (Repeat previous Dword until)
1048: - D3.7+ E3 1100011110  +D28.7- FC 0011100001  - D3.7+ E3 1100011110  +D28.7- FC 0011100001
1049: -D12.0+ 0C 0011011011  +D11.4- 8B 1101000010  -D12.0+ 0C 0011011011  +D11.3+ 6B 1101000011  LBA
1050: +D12.0- 0C 0011010100  -D11.4+ 8B 1101001101  +D12.0- 0C 0011010100  -D11.3- 6B 1101001100  LBA
                                    (Repeat previous ***2 Dwords*** until)
1281: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
1283: -D12.0+ 0C 0011011011  +D11.4- 8B 1101000010  -D12.0+ 0C 0011011011  +D11.3+ 6B 1101000011  LBA
1284: +D12.0- 0C 0011010100  -D11.4+ 8B 1101001101  +D12.0- 0C 0011010100  -D11.3- 6B 1101001100  LBA
                                    (Repeat previous ***2 Dwords*** until)
1307: -D20.2- 54 0010110101  -D20.2- 54 0010110101  -D20.2- 54 0010110101  -D20.2- 54 0010110101
                                    (Repeat previous Dword until)
1537: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
1539: -D20.2- 54 0010110101  -D20.2- 54 0010110101  -D20.2- 54 0010110101  -D20.2- 54 0010110101
                                    (Repeat previous Dword until)
1564: -D20.2- 54 0010110101  -D20.7+ F4 0010110111  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010
1565: +D11.5+ AB 1101001010  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010
                                    (Repeat previous Dword until)
1793: +K28.5- BC 1100000101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D27.3+ 7B 1101100011  ALIGN
                                    (Repeat previous Dword until)
1795: +D11.5+ AB 1101001010  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010
                                    (Repeat previous Dword until)
1822: +D11.5+ AB 1101001010  +D11.7- EB 1101001000  -D20.2- 54 0010110101  -D20.2- 54 0010110101
1823: -D21.5- B5 1010101010  -D21.5- B5 1010101010  -D21.5- B5 1010101010  -D21.5- B5 1010101010
                                    (Repeat previous Dword until)
1887: -D24.3+ 78 1100110011  +D24.3- 78 0011001100  -D24.3+ 78 1100110011  +D24.3- 78 0011001100
                                    (Repeat previous Dword until)
1951: -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101
                                    (Repeat previous Dword until)
2015: -D25.6- D9 1001100110  - D6.1- 26 0110011001  -D25.6- D9 1001100110  - D6.1- 26 0110011001
                                    (Repeat previous Dword until)
2049: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
```

```
2051: -D25.6- D9 1001100110  - D6.1- 26 0110011001  -D25.6- D9 1001100110  - D6.1- 26 0110011001
                                  (Repeat previous Dword until)
2081: -D11.6- CB 1101000110  -D18.6- D2 0100110110  -D29.6+ DD 1011100110  + D6.4- 86 0110010010
2082: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D21.6+ D5 1010100110  +D21.6+ D5 1010100110  EOF
2083: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D24.2+ 58 1100110101  +D24.2- 58 0011000101  WTRM
2084: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D24.2- 58 0011000101  -D24.2+ 58 1100110101  WTRM
2085: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D24.2+ 58 1100110101  +D24.2- 58 0011000101  WTRM
2086: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D24.2- 58 0011000101  -D24.2+ 58 1100110101  WTRM
2087: +K28.3- 7C 1100001100  -D21.4+ 95 1010101101  +D21.5+ B5 1010101010  +D21.5+ B5 1010101010  SYNC
                                  (Repeat previous Dword until)
2089: +K28.3- 7C 1100001100  -D10.5- AA 0101011010  -D25.4+ 99 1001101101  +D25.4- 99 1001100010  CONT
2090: -K28.3+ 7C 0011110011  +D10.5+ AA 0101011010  +D25.4- 99 1001100010  -D25.4+ 99 1001101101  CONT
2091: +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101
                                  (Repeat previous Dword until)
2304: +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101
```