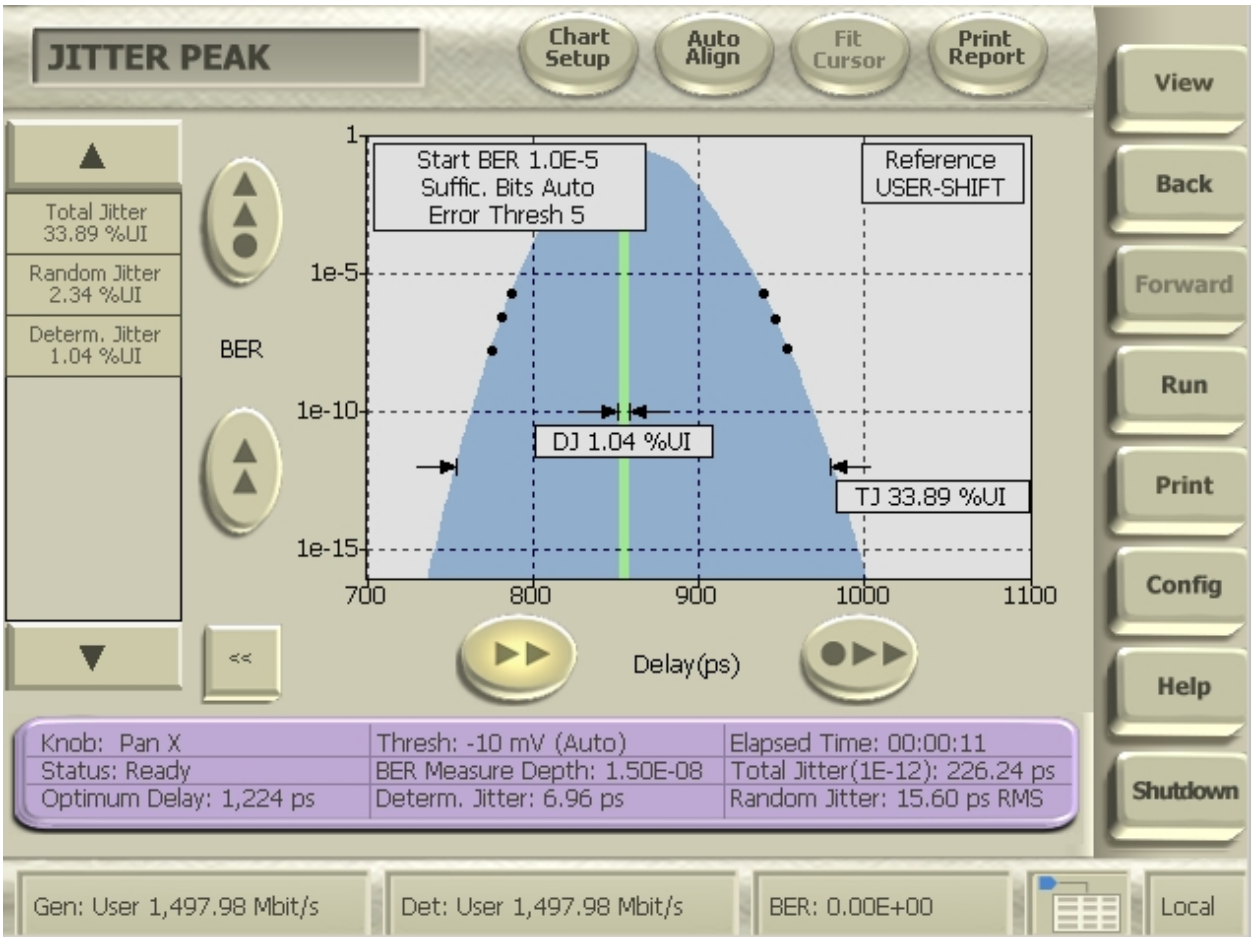
Serial ATA International Organization

Version 1.0
June 3, 2010

Serial ATA Interoperability Program Revision 1.3 SyntheSys Research, Inc. MOI for PHY, TSG & OOB Tests (using BERTScope 7500B with CR)



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MODIFICATION RECORD

First draft, January 25, 2006
Version 0.8, February 6, 2006
Version 0.93RC, March 14, 2006
Version 0.94RC, March 22, 2006: "using either the BIST T,S,A mode or other suitable method" inserted in the initiating step in PHY-01 through TSG-12. TSG01 section inserted. "Possible Issues" inserted in TSG-02. TSG04 removed one cable to improve the setup and corrected labels in step 4. TSG05 and TSG06 corrected to: "at least 10,000 samples" and "mean" Amplitude Imbalance. Inserted: "When initiating via BIST; there is 50% "in Possible Issues in TSG-09 through TSG-12. "This test requirement is only applicable to components claiming to be capable of running at 3Gb/s" inserted in TSG-11 and TSG-12. Appendix C step-by-step bullets filled in.
Version 0.96RC, March 23, 2006: Completed step 4 through 9 and observable results paragraphs of TSG01 and added "When calibrating the BERTScope clock need to be used. By clicking on "Synthesizer" the Clock frequency is set to either 1.5 Gbps or 3.0 Gbps. Clock and Data Outputs are enabled by clicking on the "Outputs On/Off" button. "to TSG-02.
Version 0.97RC, April 19, 2006: "SATAI (3.0)" corrected to "SATAI (6.0) in PHY-01 through TSG-02 and in TSG-09 and TSG-10. TSG-01 changed to minimum and maximum measured using the same method and TSG-02 merely using HFTP as described in Serial ATA Interoperability Program Unified Test Document, LogoTF_ILunified_v1_0RC2f.doc.
Version 0.98RC, June, 2006: Changed from "(6.0)" to "(1.98)" settings on the CR 12500A in PHY-01 through PHY-04. Updated TSG-01 and Appendix E. Updated PHY-01, PHY-04 and TSG-01 through TSG-03 with explicit requirements to save calibration screen shots. Updated TSG-09 and TSG-10 with TIE based methodology requirements of Unified Test Document, LogoTF_ILunified_v1_0RC2i.doc.
Version 0.99RC, June 7, 2006: Updated index to show TSG-01. Added reference to Comax H303000204 or equivalent in all sections. Detailed the scope measurements in PHY-03 and PHY-04.
Version 1.0RC, June 19, 2006: Modified SSC equations in PHY-04 to record SSC relative to $f_{nominal}$.
Version 1.05RC, September 14, 2006: Modified PHY-02 and PHY-04 to in clued the words "average over" ten SSC cycles for the measurement of frequency deviation. Added the Host Worst Case Port Identification test. Changed "device" to "product" and "DUT" to "PUT". Inserted note of LBP pattern being per ECN 018 and therefore disparity agnostic. Removed disparity verification of the LBP pattern from TSG-01 and TSG-09 through TSG-12. Allowing multiple choices of Stimulus Tools in Appendix A for initiation of the product and generation of BIST Active.
Version 1.07RC, September 20, 2006: Added calibration procedure to TSG-04.
Revision 1.1 Version 0.90, October 30, 2006: Revised title, revision and version according to new workgroup naming conventions. Updated the TJ and DJ limits for Gen1 1.5 Gb/s to follow the limits for other clock to data jitter measurements, namely 0.37 and 0.19 UI respectively.
Revision 1.1 Version 0.91, November 6, 2006 and Revision 1.1 Version 1.0RC, November 16, 2006: Changed "Revision 0.90" to "Version 0.91" and moved "Revision 1.1" on cover page, Merged PHY-02, PHY-03 and PHY-04 to share one diagram and simplify the formula for conversion from measured value to ppm. Merge TSG-09 and TSG-10 as well as TSG-11 and TSG-12 in pairs to share procedure and images.
Revision 1.1 Version 1.01RC, July 26, 2007: Added setup return loss measurement data.
Revision 1.3 Version 0.91 January 5, 2009: Added Appendix C with JTF calibration.
Added references to Jitter Transfer Function (JTF) in TSG-09 through TSG-12
Added note in OOB-02 through OOB-05 regarding +/-100 mV measurement offset.
Added calibration of signal amplitude for OOB-01 test to Appendix B
Modified PHY-02 and PHY-04 to reflect proper limits of +350, -5350 ppm
TSG-05 – corrected final formula to show two result values (per IW scorecard) rather than single value "Max" result
Moved common resource requirements and setup to Appendix E
Corrected references to SATA 2.6 Spec, and reference tables
Revision 1.3 Version 0.8 October 14, 2009: Updated Figures and down shifted revision to 0.8.
Revision 1.3 Version 0.92 March 29, 2010: Completed all Appendices and updated to 0.9 after workgroup approval.
Revision 1.0RC April 8, 2010. Moved to 1.0RC after workgroup approval.
Revision 1.0 June 3, 2010. Removed "RC" after end of 30 days review.

INTRODUCTION

These Methods of Implementations describe the step by step procedures to perform the required:

- PHY-01 through PHY-04
- TSG-01 through TSG-12 (except TSG-07 and TSG-08, which are obsolete)
- OOB-01 through OOB-07

tests of the Serial ATA Interoperability Program using the BERTScope by SyntheSys Research, Inc. in order to qualify a product for listing on the SATA Integrators List.

You will find that this MOI is a lot simpler and a lot shorter than the previous versions although it includes 7 additional OOB tests. This is due to the leverage of the new PatternVu software option which improves accuracy of amplitude, rise time and skew measurements and the inclusion of functions integrated in the latest BERTScope software.

The test setup is illustrated in Appendix E, including a simplified version of this setup for OOB tests.

The tests may be performed in sequence using automated using software shown in Test Title: Serial ATA Interop Test Suite. Please contact SyntheSys Research, Inc. at +1 (650) 364-1853 or info@bertscope.com for the availability of software and accessories.

REFERENCES

The following document is referenced in this text:

[1] Serial ATA Rersion 2.6,
[2] Serial ATA Interoperability Program Unified Test Document Revision 1_3_
[3] Serial ATA Interoperability Program Policy Document Revision 1_3_
[4] SATA_PHY_MOI_BERTScope_RSG_r13_v1.0

ACKNOWLEDGEMENTS

SyntheSys Research, Inc. would like to acknowledge the following reviewers of the earlier versions of this document:

[1] Harvey Newman, while at Infineon
[2] Jeff Choun, Marvell
[3] Jeff Wolford, HP
[4] John C. Calvin, Tektronix
[5] Mark Marlett, LSI Logic
[6] Pao-Ching Tseng, MediaTek
[7] Paschal Egan, Philips Semiconductor
[8] Serge Bedwani, Intel
[9] Steven Wong, Comax Technology

Test Title: Host Worst Port Identification

Purpose: Prior to execution of any testing on a host, a "worst port" must be identified.

Last Modification: January 5, 2009

Discussion: The intent of identifying a worst port is not to validate each port to the specification, but to simply identify the worst port based on a single relative measurement across all ports within a host. The Interoperability Tests must then be executed on the worst port identified per the procedure below.

Resource Requirements and Test Setup as shown in Appendix E

Test Procedure:

1. Power-on host and ensure test ports are enabled & functional. Run the following on each individual port.
2. Initiate the OOB-06b sequence from the BERTScope.
3. Connect the host to the SATA receptacle
4. Execute TSG-09 while the host is in NRZ idle following OOB and record results for the Total Jitter (TJ) for each port

Observable Results:

- The "worse port" is identified as that which has the highest TJ value recorded on the measurement above

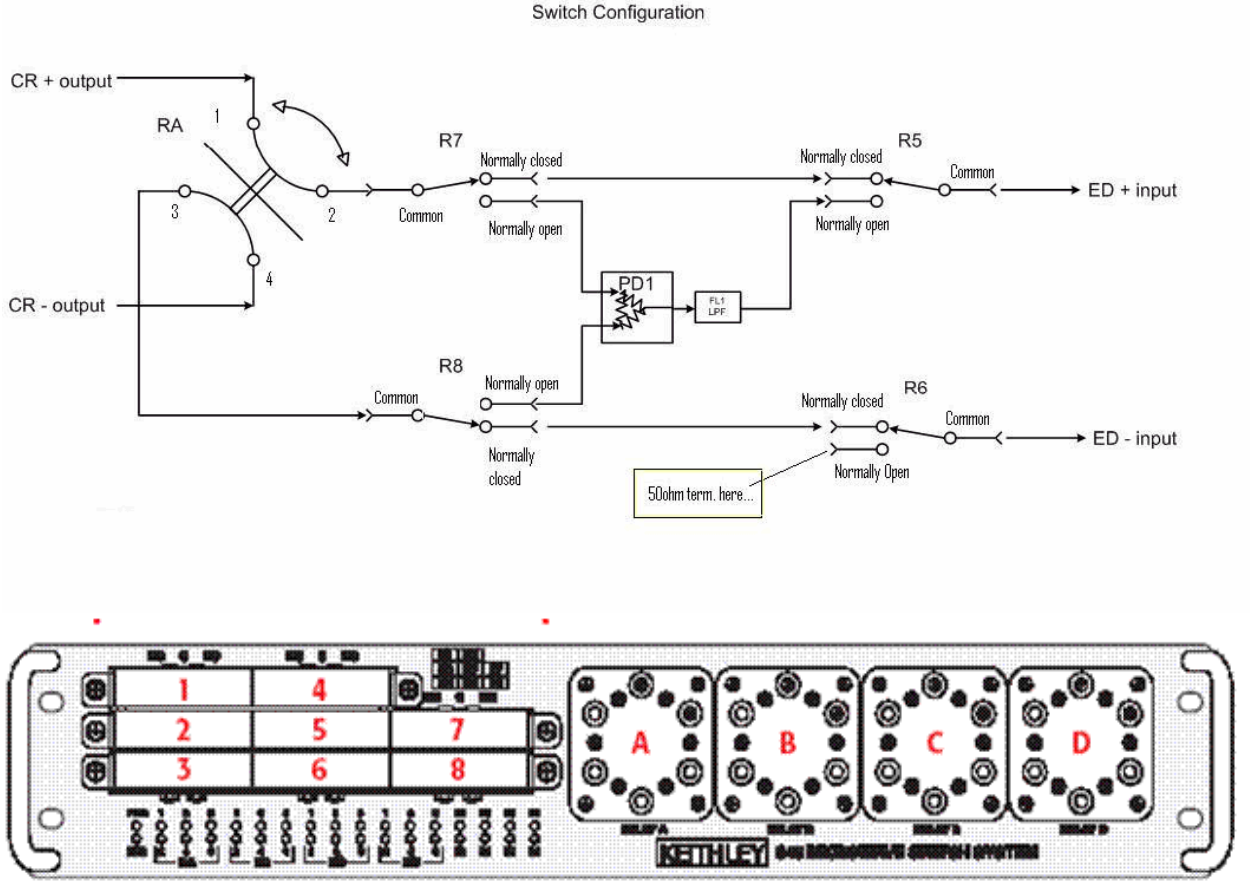
Test Title: Serial ATA Interop Test Suite Automation

Purpose: The Revision 1.3 Unified Listing tests for PHY and TSG have been automated to provide a repetitive and fast execution, namely less than 15 minutes for the Serial ATA Interop Test Suite.

Last Modification: January 5, 2009

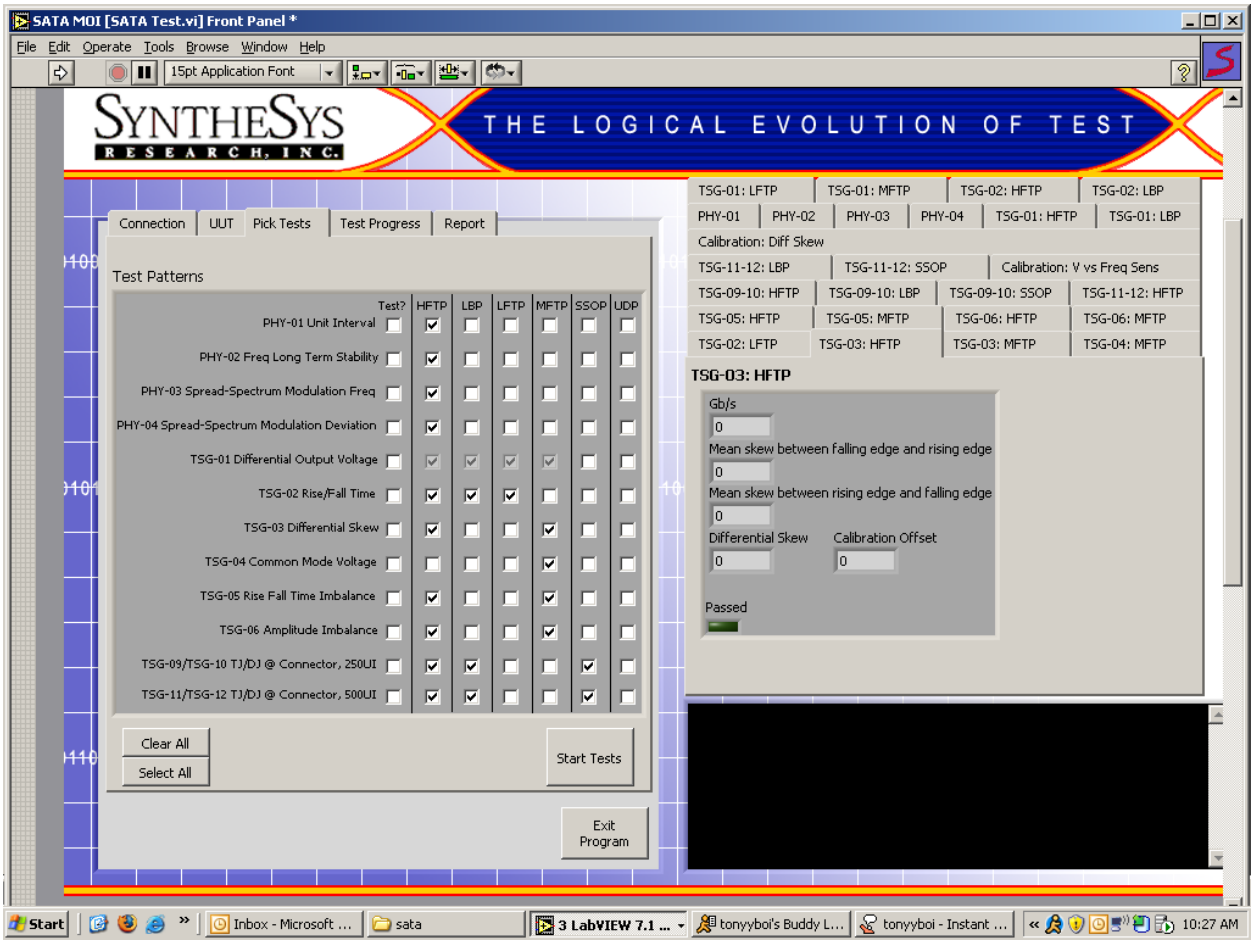
Discussion: Automation speeds up the measurements and assures repeatability by elimination human interactions. The tests are executed by use of the PC controller as they are individually described in the following Test Titles. All tests may therefore be executed manually in absence of a suitable controller. Although BIST "L" loop back is the preferred mode for the automated Test Suite, the Test Suite does allow for BIST "T,A,S" mode testing as well, The BERTScope SATA Tee Test Fixture additionally allows for testing of PUTs that do not support disconnect.

Resource Requirements and Test Setup as shown in Appendix E: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Keithley switch ports RA1 and RA4 respectively and the Keithley switch ports R5-Common and R6 Common respectively to Data Input + and – ports of the BERTScope using the matched pair of 1 meter cables as per the following Figure. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports. Connect the USB cable between the CR12500A and the BERTScope and connect the controller PC to the BERTScope via the Ethernet connection. Connect the Keithley switches to each other and to the power combiner, terminations and filter using the 7 six inch cables as per the following Figure. The Keithley switch is further connected to the controller PC via the Ethernet to GBIP converter.



Test Procedure:

1. Connect controller to the set-up and follow the Serial ATA Interop Test Suite on-screen instructions.



Observable Results:

- The observable results are recorded in an Interop spread sheet compatible format and compared against Interop test limits for pass/fail indication.

Test Title: PHY-01: Unit Interval

Purpose: Verify that the Product Under Test, PUT, meets the Unit Interval specification of section 7.2.2.1.3 of Serial ATA revision 2.6 at both 1.5 Gb/s and 3 Gb/s if the PUT claims to support both rates.

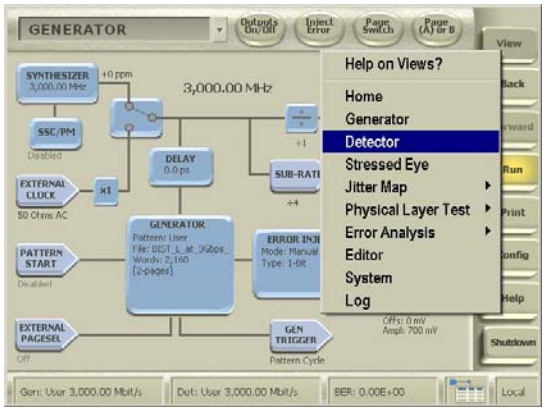
Last Modification: January 5, 2009

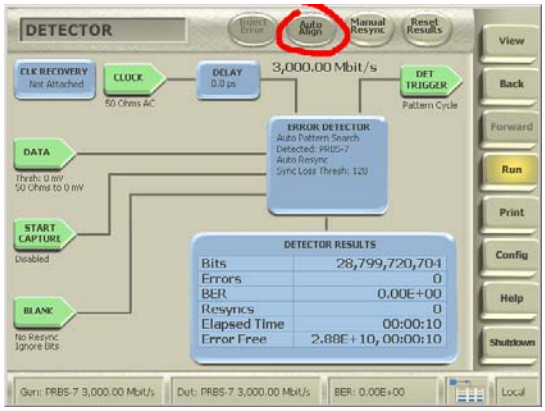
Discussion: For components which claim to support 3Gb/s, this requirement must be tested at both interface rates (1.5Gb/s and 3Gb/s). The BERTScope automatically perform the Unit Interval measurement according to section 7.2.2.1.3 of the Serial ATA revision 2.6 based on more than 100,000 UIs.

Resource Requirements and Test Setup as shown in Appendix E.

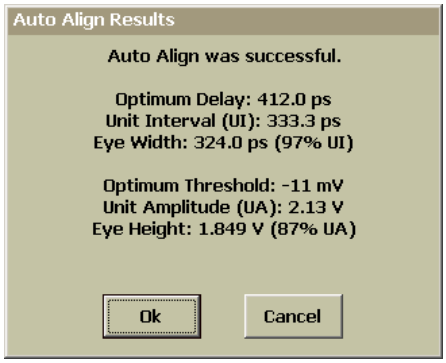
Test Procedure:

2. Initiate the PUT transmitting the HFTP pattern (D10.2) using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the PUT to the SATA receptacle
4. On CR 12500A, choose the appropriate pre-stored selection: "SATA1 (1.98)" for 1.5 Gb/s or "SATA2 (1.98)" for 3 Gb/s; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
5. On the BERTScope, Select "View" then "Detector" and click on "Auto Align".





A pop-up window will appear with the Unit Interval measurement result.



6. Record the measured Unit Interval.
7. If the PUT claim to be capable of running at 3 Gb/s then repeat 1 through 5 of above to get both 1.5 Gb/s and 3 Gb/s measurements.

Observable Results: The pass/fail criteria are:

- PHY-01a: Mean Unit Interval measured shall be between 666.4333ps (min) and 670.2333ps (max) (for components when running at 1.5Gb/s)
- PHY01b: Mean Unit Interval measured shall be between 333.2167ps (min) and 335.1167ps (max) (for components claiming to be capable of running at 3Gb/s)

Test Title: PHY-02: Frequency Long Term Stability
Test Title: PHY-03: Spread-Spectrum Modulation Frequency
Test Title: PHY-04: Spread-Spectrum Modulation Deviation

Purpose: Verify that the Product Under Test, PUT, meets the Frequency Long Term Stability specification of section 7.2.2.1.4; the Spread-Spectrum Modulation Frequency specification of section 7.2.2.1.5; and the Spread-Spectrum Modulation Deviation specification of section 7.2.2.1.6 and 7.3.3 of Serial ATA revision 2.6.

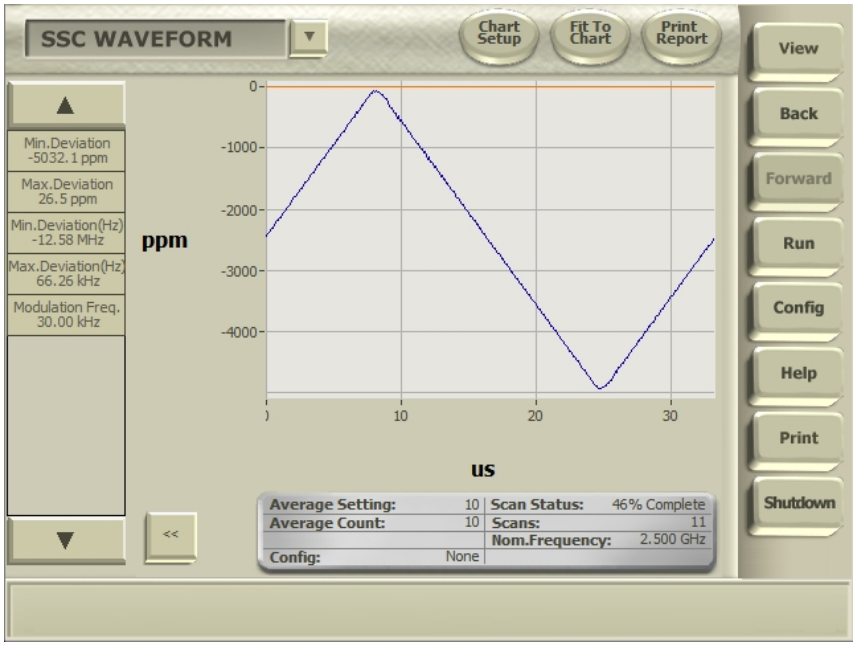
Last Modification: January 5, 2009

Discussion: These tests are only run once at the maximum interface rate claimed by the component (1.5Gb/s or 3Gb/s). PHY-02 is not applicable to PUTs that support SSC, whereas PHY-03 and PHY-04 are only run on PUTs claiming support of SSC. The BERTScope CR12500A has a built-in frequency counter that automatically performs the frequency measurement according to section 7.4.6 of the Serial ATA revision 2.6. The BERTScope CR 12500A further automatically demodulates the incoming data signal and displays the spread-spectrum modulation waveform and measures the Spread-Spectrum Repetition and Modulation Frequency over at least 10 cycles using the internal precision frequency counter according to section 7.4.11 of the Serial ATA revision 2.6.

Resource Requirements and Test Setup as shown in Appendix E.

Test Procedure:

1. Initiate the PUT transmitting the HFTP pattern (D10.2) at the highest of the 1.5 Gb/s or 3 Gb/s that the PUT claims to capable of using either the BIST T,S,A mode or other suitable method as described in Appendix A.
2. Connect the PUT to the SATA receptacle
3. On CR 12500A, choose the appropriate pre-stored selection: “SATA1 (1.98)” for 1.5 Gb/s or “SATA2 (1.98)” for 3 Gb/s; by pressing Enter, scroll to the desired setting and press “Enter” again.
4. If the PUT does not claim to support SSC then record the measured CR 12500A frequency counter measurement to ppm using the following formula: $ppm_{counter} = (f_{counter} - f_{nominal})/f_{nominal.}$ $f_{nominal}$ is 1.5 GHz for PUTs running at 1.5 Gb/s and 3 GHz for PUTs claiming to be capable of running at 3 Gb/s. Record $ppm_{counter}$ as the measured Frequency Long Term Stability for PHY-02. If the PUT claims to support SSC then skip to step 5.
5. This step provides the PHY-03 and PHY-04 measurements which are only run on PUTs claiming support of SSC. On the BERTScope select “View”, “Physical Layer Tests” then “SSC Waveform”. Click “run” and wait until the “Average Count” has reached 10. Enable the left side measurement sidebar by clicks on the “<<” and “Measurements”. Record the measured spread-spectrum Modulation Frequency (in kHz), Min. Deviation (in ppm) and Max. Deviation (in ppm) averaged over 10 cycles.



6. Record Max. Deviation (in ppm) as the measured Frequency Long Term Stability for PHY-02 and Min Deviation (in ppm) as the measured Spread Spectrum Modulation Deviation for PHY-04 if the PUT is claimed to be SSC capable.

Observable Results: The pass/fail criteria are:

- PHY-02: The measured Frequency Long Term Stability, $ppm_{counter}$ for PUT claiming not to support SSC shall be between -350 ppm and 350 ppm.
- PHY-03: The measured Spread-Spectrum Modulation Frequency shall be between 30 kHz and 33 kHz.
- PHY-04a: The measured Maximum Spread-Spectrum Modulation Deviation, Max. Deviation in ppm shall be less than +350 ppm.
- PHY-04b: The measured Minimum Spread-Spectrum Modulation Deviation, Min. Deviation in ppm shall be greater than -5350 ppm.

Test Title: TSG-01: Differential Output Voltage
Test Title: TSG-02: Rise/Fall Time

Purpose: Verify that the Product Under Test, PUT, meets the Rise and Fall Time specification of section 7.2.2.3.3 of Serial ATA revision 2.6 while transmitting the HFTP (D10.2) pattern and meets the Differential Output Voltage specification of section 7.2.2.3.3 of Serial ATA revision 2.6 while transmitting specified patterns, namely HFTP, MFTP and LBP at both 1.5 Gb/s and 3 Gb/s if the PUT claims to support both rates.

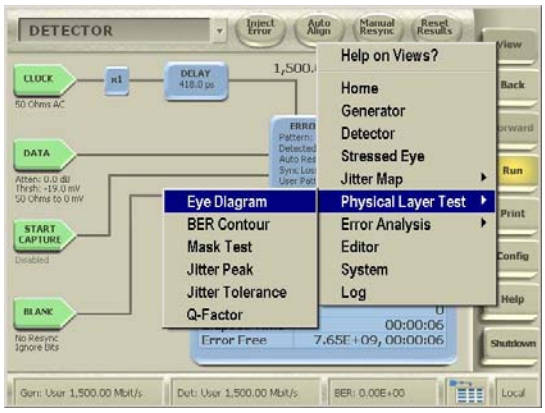
Last Modification: January 5, 2009

Discussion: For components which claim to support 3Gb/s, this requirement must be tested at both interface rates (1.5Gb/s and 3Gb/s). The BERTScope simultaneously captures the amplitudes for various bits in described set-up according to section 7.4.2 of the Serial ATA revision 2.6.

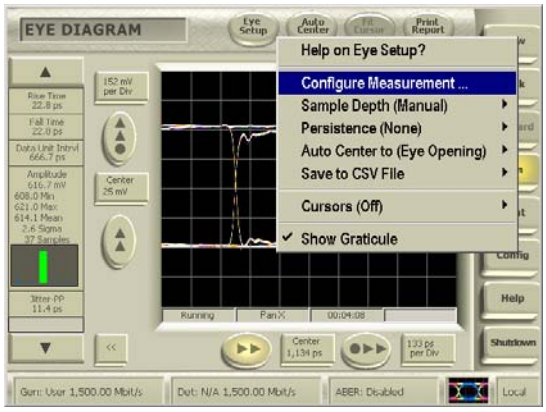
Resource Requirements and Test Setup as shown in Appendix E.

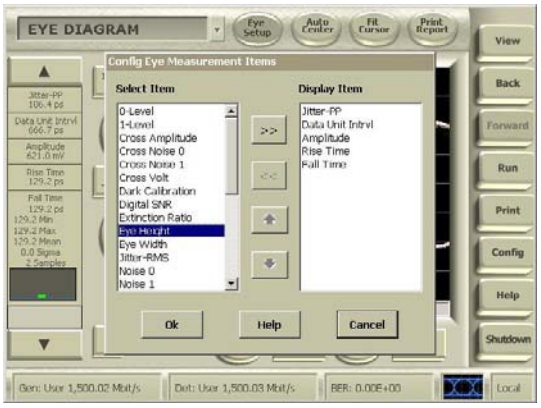
Test Procedure:

1. On CR 12500A, choose the appropriate pre-stored selection, which must first have been calibrated to provide the specified JTF function as per Appendix B: "JTF-SATA1" for 1.5 Gb/s or "JTF-SATA2" for 3 Gb/s; by pressing "Enter", scroll to the desired setting and press "Enter" again.
2. Initiate the PUT transmitting the HFTP pattern using either the BIST L (preferred) or T,S,A mode or other suitable method as described in Appendix A and Connect the PUT to the SATA receptacle
3. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center". Click "Yes" to perform delay line calibrations if prompted by a pop-up window.

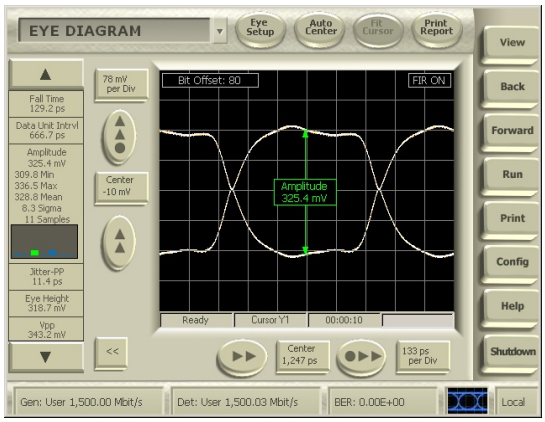


1. Click on "Eye Setup" and select "CleanEye" as the "Eye Operating Mode". Set the pattern length to "manual" and the value to "80". Enable the FIR filter as calibrated in Appendix B for the selected interface rate by clicking on "Eye Setup" then "Enable FIR"; "Configure FIR" and "Load Filter" also click "Eye Setup" "Configure Measurement" and add "Eye Height" to the measurement list by highlighting "Eye Height" then click on ">>" and "OK"
   .



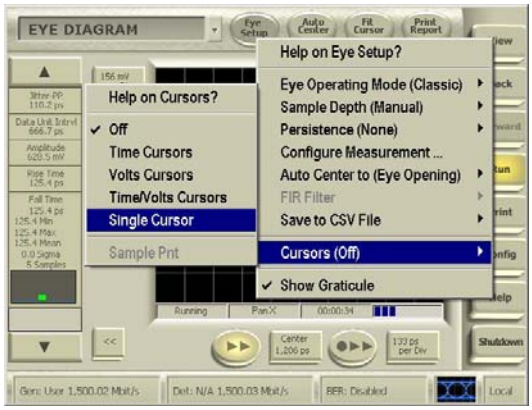


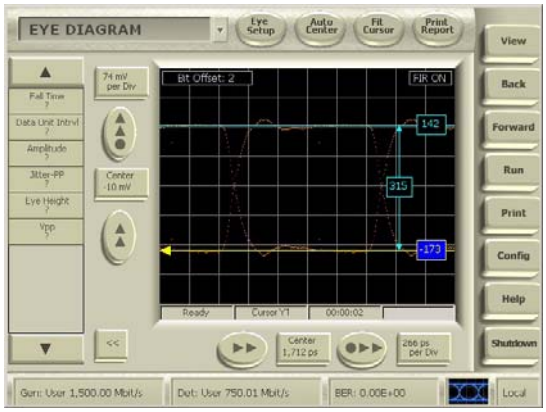
4. Click on "Run" on the right side bar to start the measurement. Enable the left side measurement sidebar by clicks on the "<<" and "Measurements". All measurements, amplitude, rise and fall time are done simultaneously and the measurement points can be see by clicking on the parameter and selecting "Detailed View" before, during or after the measurement.



More than 100,000 samples are automatically collected. The formula; 1537 $(s/x)^2 \leq n$ is therefore easily satisfied as long as the standard deviation, s, is less than 5 times amplitude x. The term (1.96 s /√ n) is less than 1% of s and can therefore be ignored when computing the value DH = [x – (1.96 s /√ n)]. Record the measure amplitude for the HFTP pattern as DH.

5. Click on the "Fall Time" measurement field on the left side bar on the BERTScope and select "Detailed View". Record the mean Fall Time value (no need to wait since the fall time measurements were done simultaneously with the rise time measurements).
6. Repeat step 5 for "Rise Time" values.
7. On the CR12500A scroll down to "SubDiv: 1", press "Enter" and scroll to select "2" and click "Enter
8. Repeat 2 through 4 with the PUT initiated transmitting the MFTP pattern and either save the csv file of the single value waveform at 20 samples per bit (the difference in values of the 15th and 35th samples is the amplitude of the MFTP) or use the cursor to measure the amplitude at the second "1" and "0" which is 0.5 UI from the center of the MFTP "1100" eye. Setting the CR subrate clock divider to divide by 2 provides an eye diagram at half the rate. Enable cursor by clicking "Eye Setup", "Cursor (Off)" and select "Voltage Cursor". The cursor can then easily be placed at the 50% point of the second of the two consecutive ones and two consecutive zeros. Record the measured amplitude for the MFTP pattern as DM





9. On the CR12500A scroll down to "SubDiv; 2", press "Enter" and scroll to select "1" and click "Enter".
10. Repeat 2 through 4 with the PUT initiated transmitting the LBP pattern this time measuring the "Eye Height" which is the amplitude of the lone bit. Record the measured eye height for the LBP pattern as VTestLBP.
11. Record the smallest value of DH, DM and VTestLBP as the minimum differential voltage, VdiffTX(Min) and the largest value of DH, DM and VTestLBP as the maximum voltage, VdiffTX(Max).
12. If the PUT claims to be capable of running at 3 Gb/s then repeat 1 through 11 of above to get both 1.5 Gb/s and 3 Gb/s measurements.

Observable Results: The pass/fail criteria are:

- The measured minimum differential voltages, VdiffTX(Min), shall both be larger than 400 mV (TSG-01a at 1.5 Gb/s as well as TSG-01g at 3.0 Gb/s for components claiming to be capable of running at 3Gb/s)
- Each of the measured maximum differential voltages, VdiffTX(Max) are recorded at 1.5 Gb/s as well as at 3.0 Gb/s for components claiming to be capable of running at 3Gb/s, but there is not any pass/fail limit.
- Each of the measured Rise, TSG-02a, and Fall, TSG-02b, Time values shall be less than 273 ps (0.41 UI) when running at 1.5Gb/s.
- The Rise, TSG-02c, and Fall, TSG-02d, Time values measured at 3 Gb/s (for components claiming to be capable of running at 3Gb/s) shall be less than 136 ps (0.41 UI)

Test Title: TSG-03: Differential Skew

Purpose: Verify that the Product Under Test, PUT, meets the Differential Skew specification of section 7.2.2.3.4 of Serial ATA revision 2.6 while transmitting various specified patterns, namely HFTP (D10.2) and MFTP.

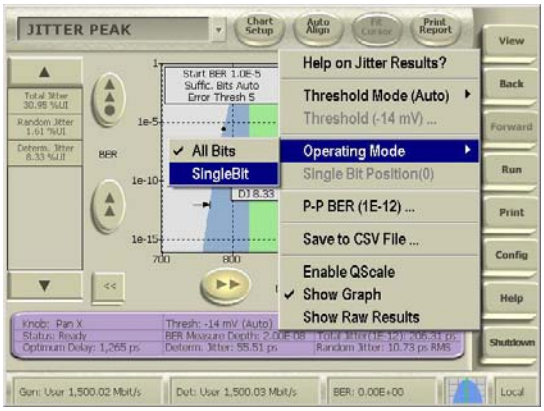
Last Modification: January 5, 2009

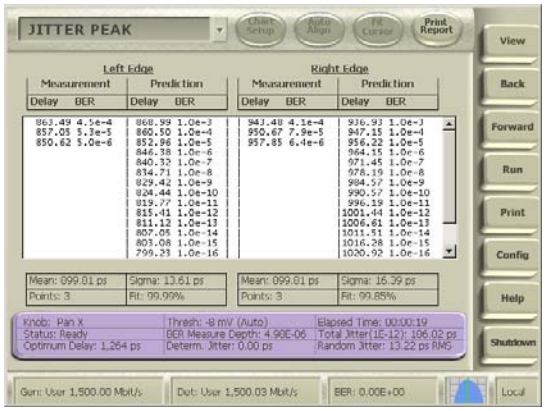
Discussion: This test is only run once at the maximum interface rate claimed by the component (1.5Gb/s or 3Gb/s). Differential skew is measured as the difference between the mean of the rising edge in a single-ended eye diagrams of TX+ and the mean of the falling edge in a single-ended eye diagram of TX–, repeat the measurement this time measuring the difference between the mean of the rising edge in a single-ended eye diagrams of TX- and the mean of the falling edge in a single-ended eye diagram of TX+, finally compute the Differential Skew = average of the magnitude (absolute value) of the two mean skews. This removes the effect of rise-fall imbalance from the skew measurement in accordance with section 7.4.12 of the Serial ATA revision 2.6.

Resource Requirements and Test Setup as shown in Appendix E: Except connect only the Data Output + port of the CR 12500A to the Data Input + port of the BERTScope using one of the matched pair of cables. Remember to terminate the other CR 12500A Data Output port and the unused BERTScope Data Input port with the 50 ohms Terminations.

Test Procedure:

1. On CR 12500A, choose the pre-stored selection: "JTF-SATA1" or "JTF-SATA2" corresponding to the highest data rate supported by the PUT; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. Initiate the PUT transmitting the HFTP pattern (D10.2) at the highest of the 1.5 Gb/s or 3 Gb/s that the PUT claims to be capable of using either the BIST L (preferred) or T,S,A mode or other suitable method as described in Appendix A.
3. Connect the PUT to the SATA receptacle.
4. On the BERTScope, select "View" then "Physical Layer Test" and "Jitter Peak" and click on the large purple bar under the image and set the "Operating Mode" to "Single Bit". Run the jitter measurement and record the average of the right side and left side mean values. This is the average crossing time of the rising edge of bit #0.





5. Click on the large purple bar to select "Bit Position (1)" and run the jitter measurement on bit position #1. Go to the "Show Raw Results" table and record the average of the right side and left side mean values. This is the average crossing time of the falling edge of bit #0 Click "No" to perform delay line calibrations if prompted by a pop-up window.
6. Move the cable from the CR 12500A Data Output + port to the CR 12500A Data Output - port. Remember to terminate the Data Output + port with the 50 ohms Termination.
7. Record the rising edge crossing and falling edge crossing times of the Data Output – port in ps by repeating steps 4 and 5 above.

8. The absolute difference between the falling level crossing of the Data Output + port and rising level crossing of the Data Output - port is the mean skew between the falling edge of Data + and the rising edge of Data -.
9. The absolute difference between the rising level crossing of the Data Output + port and falling level crossing of the Data Output - port is the mean skew between the rising edge of Data + to the falling edge of Data -.
10. Compute the Differential Skew = average of the magnitude (absolute value) of the two mean skews.
11. The skew of the matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths can be calibrated in any of two simple ways: One way is to switch the connections to the pins marked 6 and 5 of the SATA receptacle and repeat above measurements 5 through 9, the calibrated value is then the average of the two computed differential skews; the other method is to calibrate per procedure in Appendix B and subtract the calibrated setup skew from the measured differential skew. All calibration screen shots need to be saved. This is done by clicking on "Print" and select "Print to file" then create a unique file name for each calibration data including the serial number of the equipment. Additionally the skew of the SATA receptacle to SMA Female adapter, which is stated on the calibration sheet that comes with the adapter, should also be subtracted.
12. Repeat 2 through 11 with the PUT initiated transmitting the MFTP pattern on bit positions #0 and #2 (there are no transitions on bit # 1 in the MFTP pattern). Return the "Operating Mode' to "All Bits" when finished.

Observable Results: The pass/fail criterion is:

- t_{skewTX} measured shall be less than 20 ps for both HFTP, TSG-03a or b, and MFTP, TSG-03c or d, measurements.

Test Title: TSG-04: AC Common Mode Voltage

Purpose: Verify that the Product Under Test, PUT, meets the AC Common Mode Voltage specification of section 7.2.2.3.5 of Serial ATA revision 2.6 while transmitting a specified patterns, namely MFTP.

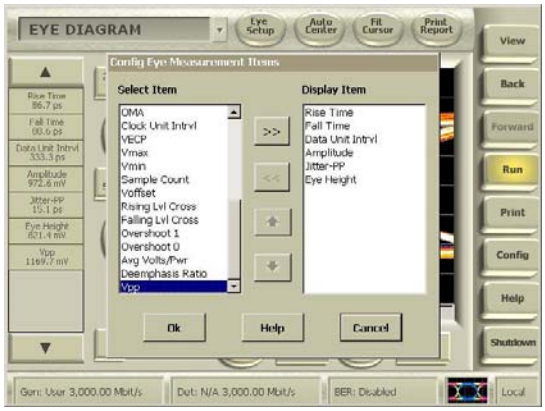
Last Modification: January 5, 2009

Discussion: This test requirement is only applicable to components claiming to be capable of running at 3Gb/s. The AC Common Mode Voltage is a measure of common mode noise other than the CM spikes during transitions due to TX+/TX- mismatch and skews which are limited by the rise/fall mismatch and other requirements. Separate channels are used for TX+ and TX- through the CR 12500A where after they are terminated in a power combiner generating common mode (TX+ + TX-) / 2. This raw common mode shall be filtered with a first order filter having a cutoff equal to the bitrate / 2 to remove the noise contribution from the edge mismatches. The peak-to-peak voltage of the filter output is the AC Common Mode Voltage and shall remain below the specified limit in accordance with section 7.4.17 of the Serial ATA revision 2.6.

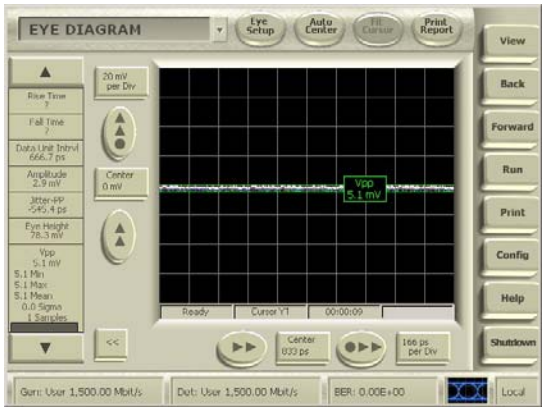
Resource Requirements and Test Setup as shown in Appendix E: Except connect the Data Output + and - ports of the CR 12500A to the symmetrical input ports of the power combiner using the matched pair of cables. Connect the output of the power combiner to the low pass filter and connect the other end of the low pass filter to the Data Input + port on the BERTScope. Terminate the Data Input – port on the BERTScope with the 50 ohms termination.

Test Procedure:

1. On CR 12500A, choose the pre-stored selection: "JTF-SATA2"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. Initiate the PUT transmitting the MFTP pattern at 3 Gb/s using either the BIST L (preferred) or T,S,A mode or other suitable method as described in Appendix A.
3. Connect the PUT to the SATA receptacle.
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram". Select "Eye Setup" then "Configure Measurement" and add "Vpp" to the list by highlighting "Vpp" then click on ">>" and "OK"



5. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram". Select "Vpp" and "Detailed View". Record the peak-to-peak voltage.



6. Multiply the peak-to-peak voltage with the calibration factor from Appendix B2. The result is the AC Common Mode Voltage.

Observable Results: The pass/fail criterion is:

- TSG-04: The measured AC Common Mode Voltage shall be less than 50 mVp-p.

Test Title: TSG-05: Rise/Fall Time Imbalance
Test Title: TSG-06: Amplitude Imbalance

Purpose: Verify that the Product Under Test, PUT, meets the Amplitude Imbalance specification of section 7.2.2.3.10 and the Rise/Fall Imbalance specification of section 7.2.2.3.9 of Serial ATA revision 2.6 while transmitting various specified patterns, namely HFTP (D10.2) and MFTP.

Last Modification: January 5, 2009

Discussion: This test requirement is only applicable to components claiming to be capable of running at 3Gb/s. In order to determine the imbalance, the single ended amplitudes and, the single ended 20-80% rise and fall times of both TX+ and TX- shall be determined for a given pattern. The amplitude imbalance value for that pattern is then calculated by the equation:

absolute value (TX+amplitude – TX-amplitude)/average, where average is (TX+amplitude + TX-amplitude)/2

where all amplitudes are determined according to section 7.4.15 of the Serial ATA revision 2.6.
Two rise/fall time imbalance values for that pattern are then determined by the two equations:

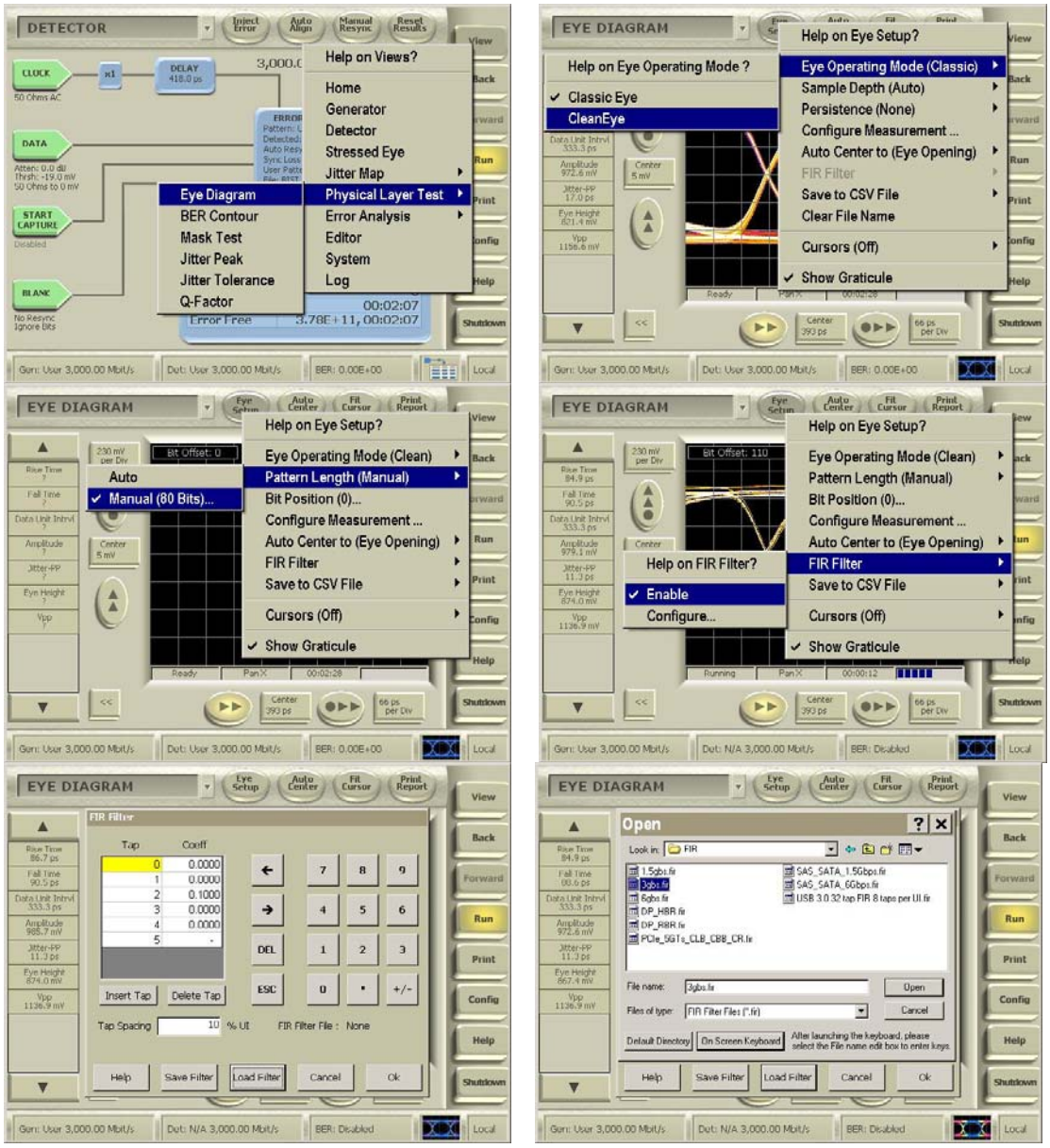
absolute value(TX+,rise – TX-,fall)/average, where average is (TX+,rise + TX-,fall)/2
absolute value(TX+,fall – TX-,rise)/average, where average is (TX+,fall + TX-,rise)/2

according to section 7.4.16 of the Serial ATA revision 2.6.

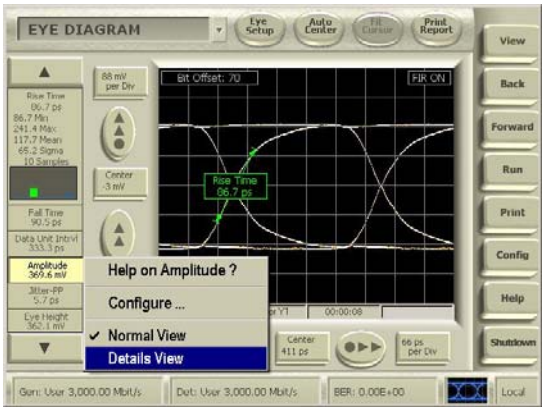
Resource Requirements and Test Setup as shown in Appendix E: Except connect only the Data Output + port of the CR 12500A to the Data Input + port of the BERTScope using one of the matched pair of cables. Remember to terminate the other CR 12500A Data Output port with the 50 ohms Termination.

Test Procedure:

1. On CR 12500A, choose the pre-stored selection: “JTF-SATA2”; by pressing “Enter”, scroll to the desired setting and press “Enter” again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to “SubDiv: 4” press “Enter” select “1” and press “Enter” again.
2. Initiate the PUT in BIST L (preferred) or T,S,A mode transmitting the HFTP pattern (D10.2) at 3 Gb/s using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the PUT to the SATA receptacle.
4. On the BERTScope, select “View” then “Physical Layer Test” and “Eye Diagram” and select “CleanEye” as the “Eye Operating Mode”. Set the pattern length to “manual” and the value to “80”. Enable the FIR filter as calibrated in Appendix B for the selected interface rate by clicking on “Eye Setup” then “Enable FIR”; “Configure FIR” and “Load Filter”.



5. Click on "Auto Center". Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Right click on the "Amplitude" measurement field on the left side bar and select "Detailed View". CleanEye automatically averages more than 10,000 samples. Record the mode amplitude and the rise and fall time values of TX+.



6. Move the cable from the CR 12500A Data Output + port to the CR 12500A Data Output - port. Remember to terminate the Data Output + port with the 50 ohms Termination.
7. Repeat 4 through 5.measuring the Amplitude of TX–.
8. Compute the imbalance value for the pattern determined by the equation: absolute value of (TX+amplitude – TX-amplitude)/average, where average is (TX+amplitude + TX-amplitude)/2
9. Compute the two imbalance values for the pattern determined by the two equations:

   absolute value(TX+,rise – TX-,fall)/average, where average is (TX+,rise + TX-,fall)/2
   absolute value(TX+,fall – TX-,rise)/average, where average is (TX+,fall + TX-,rise)/2.

10. Repeat 2 through 8 with the PUT initiated transmitting the MFTP pattern.

Observable Results: The pass/fail criterion is:

- The mean Amplitude Imbalances measured shall be less than 10% for both HFTP, TSG-05a and b, and MFTP, TSG-05c and d, measurements.
- Each pair of the two Rise/Fall Time Imbalances measured shall be less than 20% for both HFTP, TSG-06a, and MFTP, TSG-06b, measurements.

Test Title: TSG-09: TJ at Connector, Data, $f_{BAUD}/500$
Test Title: TSG-10: DJ at Connector, Data, $f_{BAUD}/500$

Purpose: Verify that the Product Under Test, PUT, meets the TJ specification of section 7.2.2.3.11 and 7.3 of Serial ATA revision 2.6 while transmitting various specified patterns, namely HFTP (D10.2), LBP and optionally if test time permits SSOP at 1.5 Gb/s.

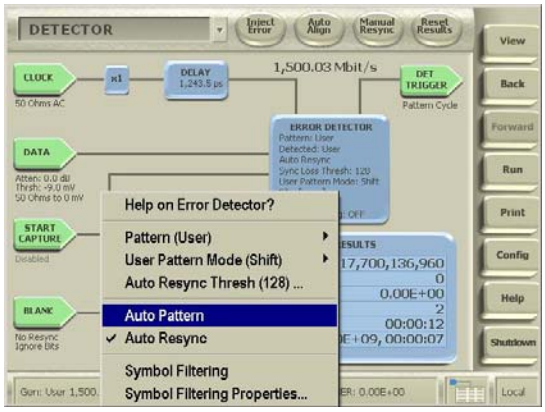
Last Modification: January 5, 2009

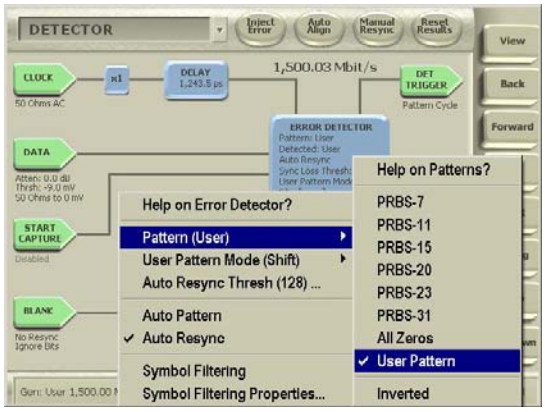
Discussion: For components which claim to support 3 Gb/s, this requirement must be tested at 1.5 Gb/s. The BERTScope simultaneously measures the TJ and DJ for TSG-09 and TSG-10 using the BERT method according to section 7.4.8 of the Serial ATA revision 2.6 using the methodology required by the following text of the Serial ATA Interoperability Program Unified Test Document: "For this test, the methodology of obtaining the results must follow a filtered TIE based method, similar to that for obtaining results for TSG-11 and TSG-12. In the past, an N-cycle method was used but is no longer preferred for the use of the interoperability testing."

Resource Requirements and Test Setup as shown in Appendix E.

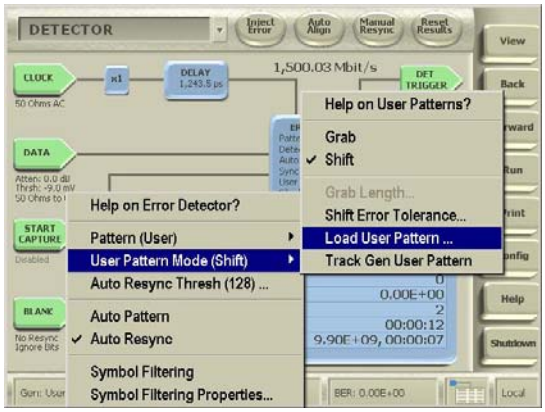
Test Procedure:

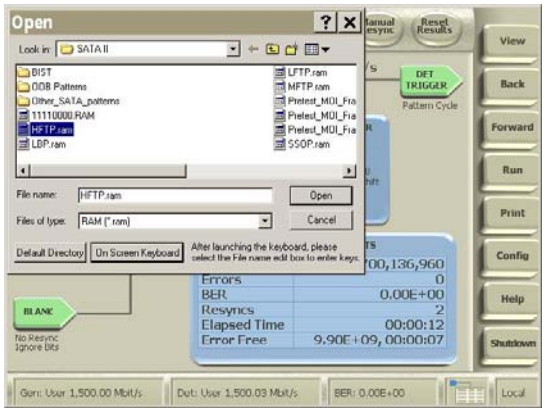
1. On CR 12500A, choose the pre-stored selection: "JTF-SATA1"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. On the BERTScope, select "View" then "Detector". Click on "Error Detector", deselect "Auto Pattern". Click on "Error Detector" again, select "Pattern" and click on "User Pattern".



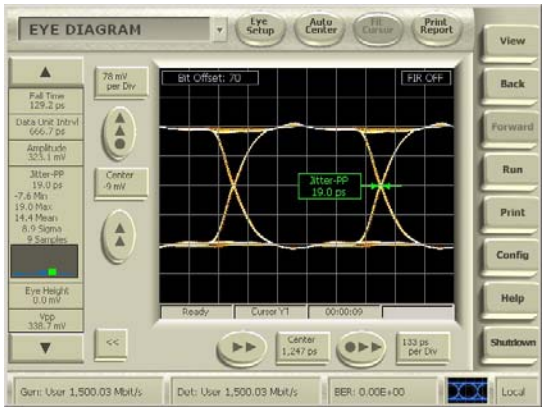


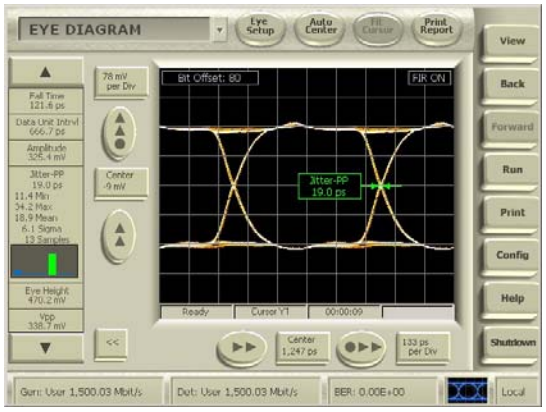
3. Click on "Error Detector" a third time, select "User Pattern Mode" and click on "Shift". Click a fourth time on "Error Detector", select "Load User Pattern" and select the HFTP pattern.



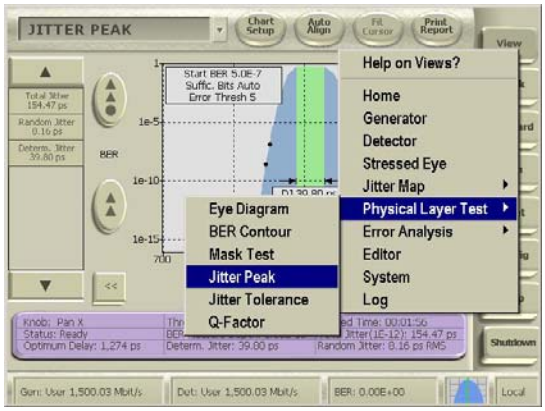


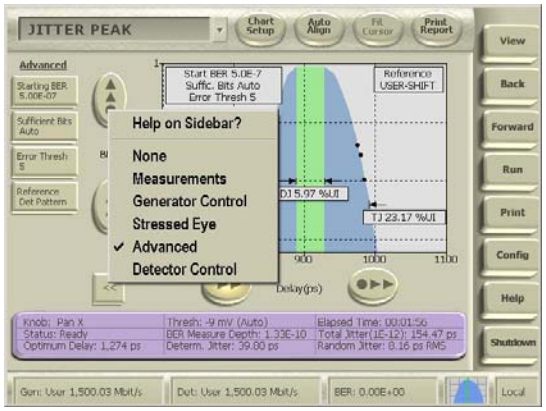
4. Initiate the PUT transmitting the HFTP pattern using either the BIST L (preferred) or T,S,A mode or other suitable method as described in Appendix A.
5. Connect the PUT to the SATA receptacle
6. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram", select "CleanEye" and click on "Auto Align" Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Set the pattern length to "manual" and the value to "80", Click run and record the jitter value, this is Data Dependent Jitter. Make a measurement with the FIR off. Select and turn-on the FIR filter as calibrated in Appendix B for the selected interface rate by clicking on "Eye Setup" then "Enable FIR"; "Configure FIR" and "Load Filter". Calculate the difference between the Jitter measured with FIR off and FIR on. The difference is the de-embedded jitter caused by cables etc. to be de-embedded from other jitter measurements.



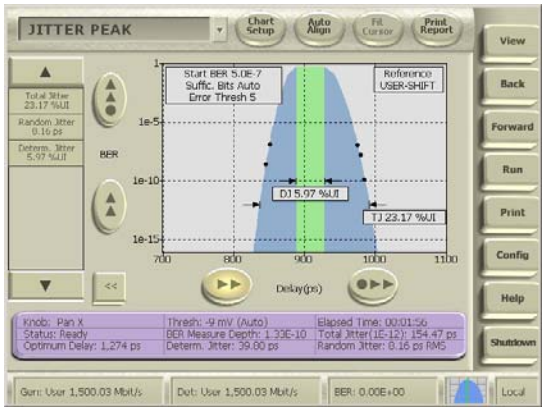


7. On the BERTScope, select "View" then "Physical Layer Test" and "Jitter Peak" and click on "Auto Align". Click the "<<" then "Advanced" to set the "Starting BER" to "5.0E-7". "Error Threshold" defaults to "5". It can be set to lower values for faster testing if desired.

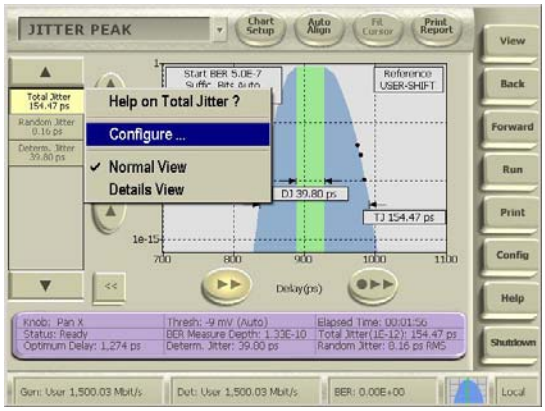


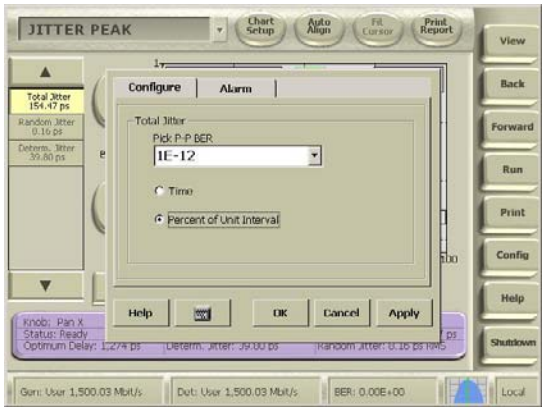


8. Wait until at least three points has been measured on each side of the Jitter Peak and record the TJ and DJ values in UI. Subtract the de-embedded jitter from both TJ and DJ to get the final TJ and DJ values.



The measurement units can be altered from pico seconds to UI by right click on “Total Jitter” on the left side bar; then click on “Configure”, select “Percentage Unit Interval”, click “OK”.





9. Repeat 4 through 6 with the LBP pattern loaded in the detector and the PUT initiated transmitting the LBP pattern.
10. Optionally repeat 4 through 6 with the PUT initiated transmitting the SSOP pattern.

Observable Results: The pass/fail criteria are:

- TSG-09a and b: TJ measured must be less than 0.37 UI at 1.5 Gb/s for each of the test patterns.
- TSG-10a and b: DJ measured must be less than 0.19 UI at 1.5 Gb/s for each of the test patterns.

Test Title: TSG-11: TJ at Connector, Clock, 500
Test Title: TSG-12: DJ at Connector, Clock, 500

Purpose: Verify that the Product Under Test, PUT, meets the TJ specification of section 7.2.2.3.12 and 7.3 of Serial ATA revision 2.6 while transmitting various specified patterns, namely HFTP (D10.2), LBP and optionally if test time permits SSOP at 3 Gb/s.

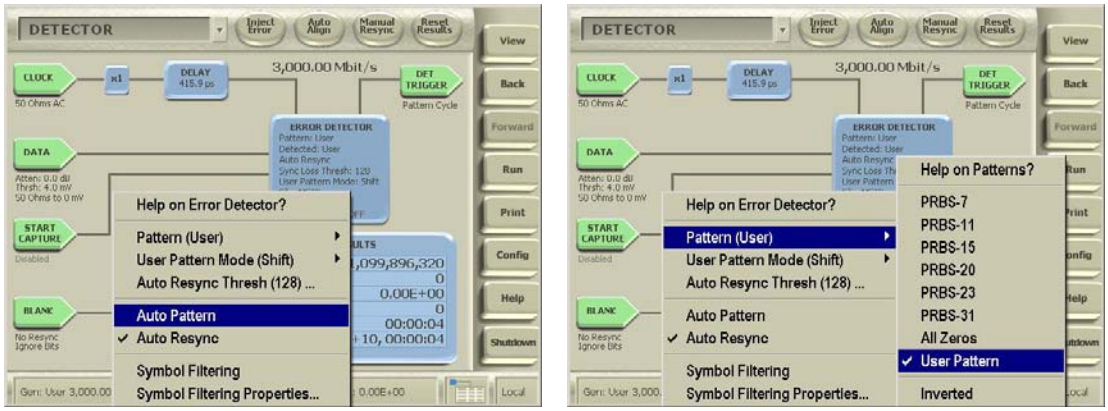
Last Modification: January 5, 2009

Discussion: This test requirement is only applicable to components claiming to be capable of running at 3Gb/s. The BERTScope simultaneously measures the TJ and DJ for TSG-11 and TSG-12 using the BERT method according to sections 7.4.6 and 7.4.8 of the Serial ATA revision 2.6.

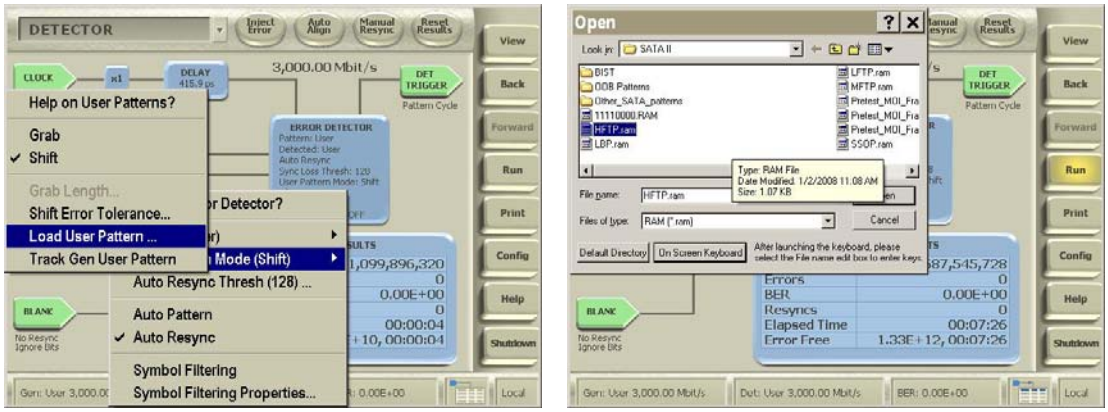
Resource Requirements and Test Setup as shown in Appendix E.

Test Procedure:

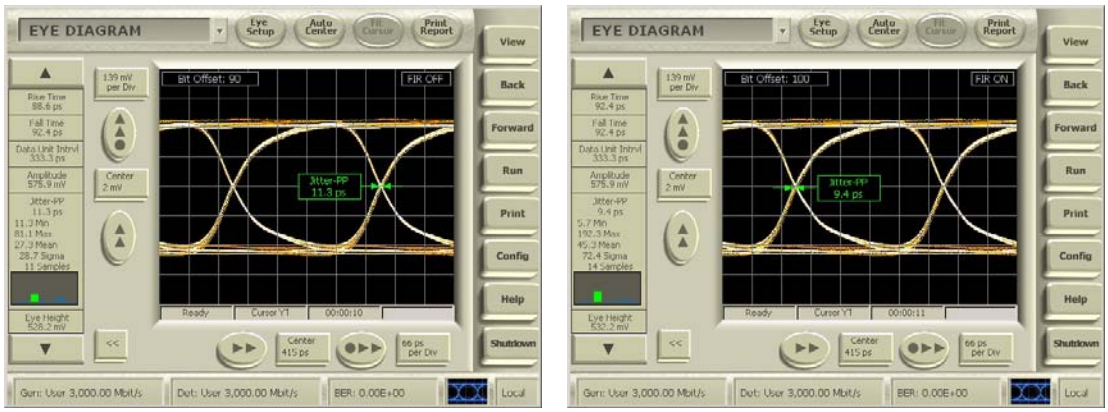
1. On CR 12500A, choose the pre-stored selection: "JTF-SATA2"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. On the BERTScope, select "View" then "Detector". Click on "Error Detector", deselect "Auto Pattern". Click on "Error Detector" again, select "Pattern" and click on "User Pattern".



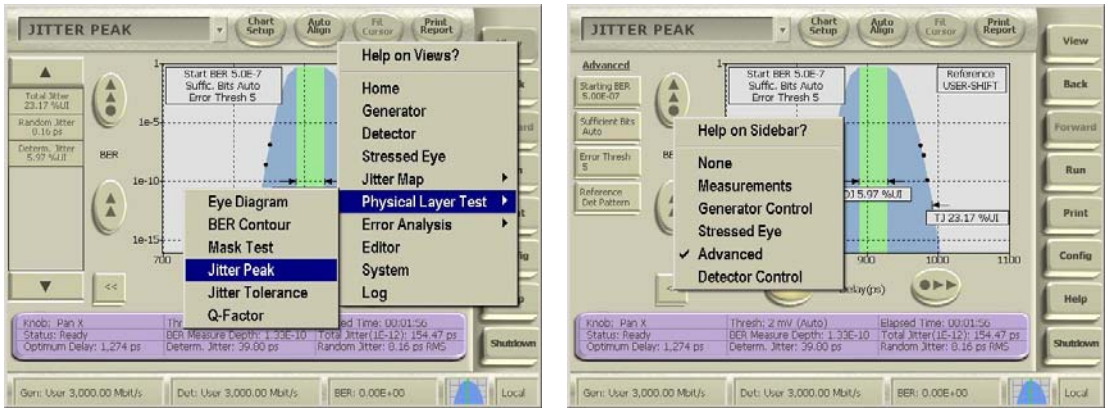
3. Click on "Error Detector" a third time, select "User Pattern Mode" and click on "Shift". Click a fourth time on "Error Detector", select "Load User Pattern" and select the HFTP pattern.



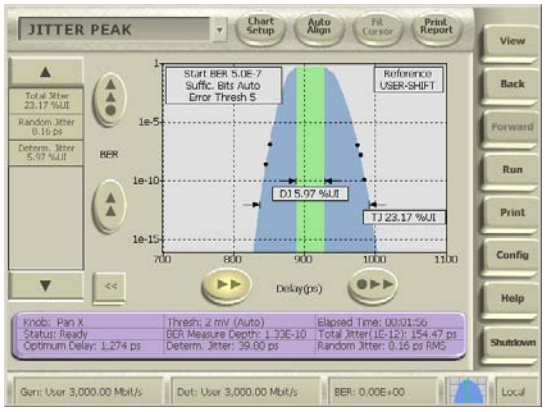
4. Initiate the PUT transmitting the HFTP pattern at 3 Gb/s using either the BIST L (preferred) or T,S,A mode or other suitable method as described in Appendix A.
5. Connect the PUT to the SATA receptacle
6. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram", select "CleanEye" and click on "Auto Align" Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Set the pattern length to "manual" and the value to "80", Turn-on the Jitter measurement and record the jitter value, this is Data Dependent Jitter. Make a measurement with the FIR off. Select and turn-on the FIR filter as calibrated in Appendix B for the selected interface rate by clicking on "Eye Setup" then "Enable FIR"; "Configure FIR" and "Load Filter". Calculate the difference between the Jitter measured with FIR off and FIR on. The difference is the de-embedded jitter caused by cables etc. to be de-embedded from other jitter measurements.



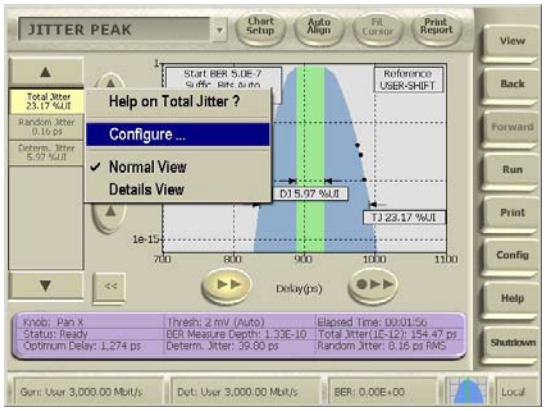
7. On the BERTScope, select "View" then "Physical Layer Test" and "Jitter Peak" and click on "Auto Align". Click the "<<" then "Advanced" to set the "Starting BER" to "5.0E-7". "Error Threshold" defaults to "5". It can be set to lower values for faster testing if desired.

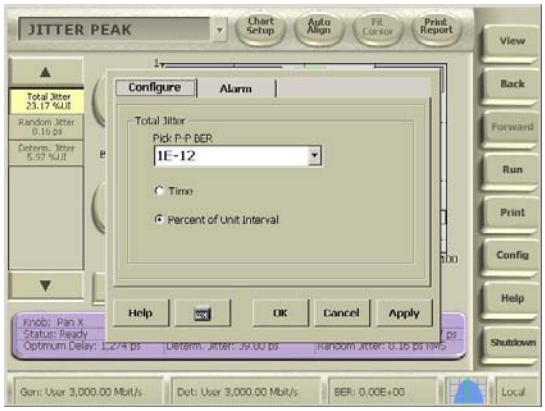


8. Wait until at least three points has been measured on each side of the Jitter Peak and record the TJ and DJ values in UI. Subtract the de-embedded jitter from both TJ and DJ to get the final TJ and DJ values.



The measurement units can be altered from pico seconds to UI by right click on “Total Jitter” on the left side bar; then click on “Configure”, select “Percentage Unit Interval”, click “OK”.





9. Repeat 4 through 6 with the LBP pattern loaded in the detector and the PUT initiated transmitting the LBP pattern.
10. Optionally repeat 4 through 6 with the PUT initiated transmitting the SSOP pattern.

Observable Results: The pass/fail criteria are:

- TSG-11a and b: TJ measured must be less than 0.37 UI at 3 Gb/s for each of the test patterns.
- TSG-12a and b: DJ measured must be less than 0.19 UI at 3 Gb/s for each of the test patterns.

Test Title: OOB-01: OOB Signal Detection Threshold

Purpose: Verify that the Product Under Test, PUT, meets the OOB Signal Detection Threshold specification of section 7.2.2.7.1 and 7.4.20 of Serial ATA revision 2.6.

Last Modification: October 30, 2008

Discussion: This test requirement must be tested at both data rates 1.5 Gb/s and 3.0 Gb/s for PUTs claiming to be capable of running at 3Gb/s. The BERTScope transmits the COMRESET/COMINT sequence of 6 COMRESET/COMINIT bursts with 480 UI gaps followed by a 45,000 UI gap and captures the 2 ms response for analysis according to sections 7.4.20 and 7.4.8 of the Serial ATA revision 2.6.

The amplitude of the COMRESET/COMINIT burst is set for 210 mV and respectively 40 mV for 1.5 Gb/s and 60 mV for PUTs claiming to support 3 Gb/s. The PUT is expected to respond to the 210 mV burst and not respond to respectively the 40 mV or the 60 mV bursts.

Resource requirements and setup for OOB are shown in Appendix E.

Test Procedure:

1. On BERTScope select "View" then "Generator" set the "Synthesizer" to 1.5 GHz and click on the "Clock Output" icon to enable these at full rate (divide by 1),
2. Click on "Pattern", deselect "Track Detector Pattern" and click on "User Pattern" to select user pattern. Then click on "Pattern" and "Load User Pattern" to select the OOB-01_COMRESET pattern from the SATA library.
3. Connect the PUT to the SATA receptacle
4. Initially enable the Data Output + (unlink and disable the Data Output – port) at V_{low} equal 0 V and V_{high} equal 1.4 V which will provide approximately 210 mV at the PUT. The amplitude must be verified during initial calibration by connecting to the BERTScope data input port.
5. On the BERTScope, select "View" then "Editor" and "File" and click on "Capture by Length". Enter the length equivalent to 5 times the OOB-01_COMRESET pattern, i.e. enter 30,525 words, which correspond to longer than 2 ms when prompted. Wait until data has been collected. Scroll down to see if the PUT repeatable responded with a correct COMINIT device or COMWAKE (host) each of which are 6 bursts of 160 UI of either 1010 or Align with respectively 480 UI or 160 UI of gaps.

```
ASSIGN WIDTH 32
%
0x00000000      0x00000000      0x00000000      0x00000000      %       0
0x00000000      0x00000000      0x00000000      0x00000000      %       4
0x00000000      0x00000000      0x00000000      0x00000000      %       8
0x00000000      0x00000000      0x00000000      0x00000000      %      12
0x00000000      0x00333333      0x33333333      0x33333333      %      16
0x33333333      0x33333333      0x33000000      0x00000000      %      20
0x00000000      0x00000000      0x00000000      0x00000000      %      24
0x00000000      0x00000000      0x00000000      0x00000000      %      28
0x00000000      0x00000000      0x00000000      0x00000000      %      32
0x00000000      0x00333333      0x33333333      0x33333333      %      36
0x33333333      0x33333333      0x33000000      0x00000000      %      40
0x00000000      0x00000000      0x00000000      0x00000000      %      44
0x00000000      0x00000000      0x00000000      0x00000000      %      48
0x00000000      0x00000000      0x00000000      0x00000000      %      52
0x00000000      0x00222222      0x22222266      0x66666666      %      56
0x66666666      0x66666666      0x66000000      0x00000000      %      60
0x00000000      0x00000000      0x00000000      0x00000000      %      64
0x00000000      0x00000000      0x00000000      0x00000000      %      68
0x00000000      0x00000000      0x00000000      0x00000000      %      72
0x00000000      0x00666666      0x66666666      0x66666666      %      76
0x66666666      0x66666666      0x66000000      0x00000000      %      80
0x00000000      0x00000000      0x00000000      0x00000000      %      84
0x00000000      0x00000000      0x00000000      0x00000000      %      88
0x00000000      0x00000000      0x00000000      0x00000000      %      92
0x00000000      0x00666666      0x66666666      0x66666666      %      96
0x66666666      0x66666666      0x66000000      0x00000000      %     100
0x00000000      0x00000000      0x00000000      0x00000000      %     104
0x00000000      0x00000000      0x00000000      0x00000000      %     108
0x00000000      0x00000000      0x00000000      0x00000000      %     112
0x00000000      0x00666666      0x66666666      0x66666666      %     116
0x66666666      0x66666666      0x66000000      0x00000000      %     120
0x00000000      0x00000000      0x00000000      0x00000000      %     124
0x00000000      0x00000000      0x00000000      0x00000000      %     128
0x00000000      0x00000000      0x00000000      0x00000000      %     132
0x00000000      0x00000000      0x00000000      0x00000000      %     136
0x00000000      0x00000000      0x00000000      0x00000000      %     140
0x00000000      0x00000000      0x00000000      0x00000000      %     144
0x00000000      0x00000000      0x00000000      0x00000000      %     148
0x00000000      0x00000000      0x00000000      0x00000000      %     152
0x00000000      0x00000000      0x00000000      0x00000000      %     156
0x00000000      0x00000000      0x00000000      0x00000000      %     160
```

6. Repeat step 6 above with the Data Outputs set at the desired amplitudes which provide respectively 40 mV and 60 mV (if the PUT claims to support 3 Gb/s) at the PUT. The PUT is not expected to respond to the test with low amplitudes. In case the PUT supports asynchronous signal recovery (ASR), it is possible that the PUT may transmit COMINIT pro-actively and not in direct response to COMRESET. Therefore if a response is recorded in step 7 then repeat step 6 at both high and low amplitudes to determine that the COMINIT is in response to the COMRESET sent by the BERTScope.

Observable Results: The pass/fail criteria are:

- For products running at 1.5Gb/s:
  - OOB-01a - Verification of no product COMINIT/COMRESET detection at 40mV
  - OOB-01b - Verification of product COMINIT/COMRESET detection at 210mV
  - If any of the above cases fails, this is considered a failure by the product.
- For products running at 3Gb/s:
  - OOB-01c - Verification of no product COMINIT/COMRESET detection at 60mV
  - OOB-01d - Verification of product COMINIT/COMRESET detection at 210mV
  - If any of the above cases fails, this is considered a failure by the product.

Test Title: OOB-02: UI During OOB Signaling
Test Title: OOB-03: COMINIT/COMRESET and COMWAKE Transmit Burst Length

Purpose: Measure the UI during OOB Signaling and verify that the Product Under Test, PUT, return COMINIT/COMRESET and COMWAKE with correct transmit burst length during OOB Signaling specification of section 7.2.2.7.2, 7.2.2.7.3 and 7.4.21 of Serial ATA revision 2.6.

Last Modification: October 30, 2008

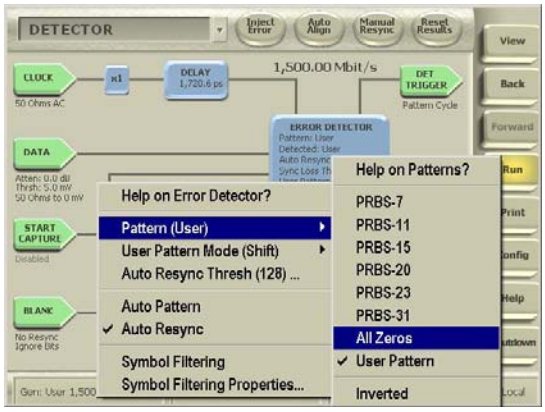
Discussion: This test requirement is only tested at the maximum data rates 1.5 Gb/s and 3.0 Gb/s for PUTs claiming to be capable of running. The BERTScope transmits the COMRESET/COMINT sequence of 6 COMRESET/COMINIT 160 UI bursts with 480 UI gaps followed by a 45,000 UI gap and captures the 2 ms response for analysis according to sections 7.4.11 and 7.4.21 of the Serial ATA revision 2.6.

The COMINIT/COMRESET and COMVAKE transmit burst length are measured at +100 mV and -100 mV offsets. There are four different patterns allowed for OOB signaling; namely Align with positive or negative disparity and D24.3 with positive or negative disparity.

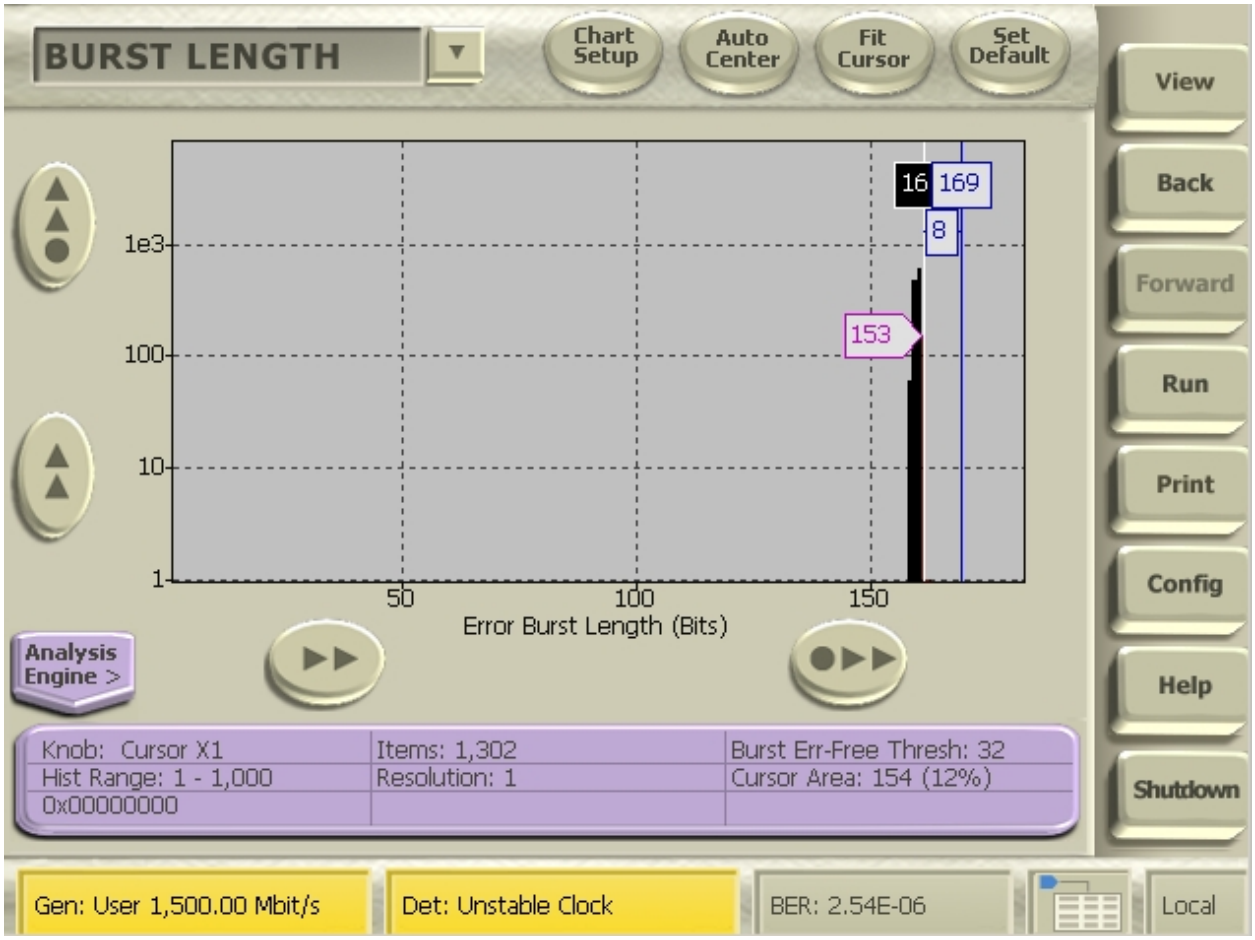
Resource requirements and setup for OOB are shown in Appendix E.

Test Procedure:

1. On BERTScope select "View" then "Generator" set the "Synthesizer" to 1.5 GHz and click on the "Clock Output" icon to enable these at full rate (divide by 1),
2. Click on "Pattern", deselect "Track Detector Pattern" and click on "User Pattern" to select user pattern. Then click on "Pattern" and "Load User Pattern" to select the OOB-01_COMRESET pattern from the SATA library.
3. Connect the PUT to the SATA receptacle
4. Enable the Data Output + (unlink and disable the Data Output – port) at V_{low} equal 0 V and V_{high} equal 2 V which will provide approximately 300 mV at the PUT.
5. On the BERTScope, select "View" then "Detector". Click on "Error Detector", click on "Pattern (User)" and select and select the "All_Zeros" pattern. . Click "Yes" to perform delay line calibrations if prompted by a pop-up window.



6. Select the "Eye Diagram" view. Click on "Configure" and choose "Cursors" Select the "Single Cursor" and set it at 100 mV in the center of the eye. Stop the Eye Diagram from running. Click on "Configure" and "Cursors" again and choose the cursor to be the "Sampling Point"
7. Switch to "View" "Error Location Analysis" and select "BER" Set the "Burst Error Free Threshold to 32. Then proceed to run "Burst Error Length" view. Stop the run when the resulting histogram shows the distribution of at least 10 (minimum 5 COMINIT/COMRESET and 5 COMVAKE) OOB-03 burst lengths relative to the 666.666 ps Unit Interval (UI) at the nominal 1.5 Gb/s rate.



8. Use the "Bit Cursors" from "Chart Setup" to record the number of hits per burst length. Calculate the mean of the burst length (in UI).
9. Repeat steps 6 through 8 above but with the threshold set to -100 mV and the detector pattern inverted so that it becomes "all ones".
10. Calculate the average of the burst lengths measured at +100 mV and -100 mV and multiply with the normalized UI namely 0.675106 ns (which takes into account that the average of the burst lengths measured at +100 mV and -100 mV is 158 UI) to get the burst length of the PUT in ns for the OOB-03 measurement.
11. Divide the burst length obtained in step 10 by 160 to get the Unit Interval during OOB for the OOB-02 measurement.
12. Hosts respond to the COMINIT plus COMVAKE test pattern by returning only a COMVAKE. It is therefore necessary to make one more measurement for hosts. Most hosts asynchronously send the COMRESET bursts for these it is easy to merely repeat steps 6 through 8 above but without sending the OOB test pattern to the host. All hosts send the COMRESET when the hosts first boots. The technique in OOB-01 can therefore be used for all other hosts to capture the COMRESET from the hosts and count the average burst length.

Observable Results: The pass/fail criteria are:

OOB-02:

- Mean UI_{OOB} measured to be between 646.67 ps and 686.67 ps over entire OOB burst

OOB-03:

- Burst Length measured to be between 103.5 ns and 109.9 ns

Test Title: OOB-04: COMINIT/COMRESET Transmit Gap Length
Test Title: OOB-05: COMWAKE Transmit Gap Length

Purpose: Verify that the Product Under Test, PUT, return COMINIT/COMREST and COMWAKE with correct gap length during OOB Signaling specification of section 7.2.2.7.4, 7.2.2.7.5 and 7.4.21 of Serial ATA revision 2.6.

Last Modification: March 9, 2009

Discussion: This test requirement is only tested at the maximum data rates 1.5 Gb/s and 3.0 Gb/s for PUTs claiming to be capable of running. The BERTScope transmits the COMRESET/COMINT sequence of 6 COMRESET/COMINIT 160 UI bursts with 480 UI gaps followed by a 45,000 UI gap and captures the 2 ms response for analysis according to sections 7.4.2.1 of the Serial ATA revision 2.6.

The COMINIT/COMRESET and COMVAKE transmit gap length are measured at +100 mV and -100 mV offsets.

Resource requirements and setup for OOB are shown in Appendix E.

Test Procedure:

1. On BERTScope select "View" then "Generator" set the "Synthesizer" to 1.5 GHz and click on the "Clock Output" icon to enable these at full rate (divide by 1),
2. Click on "Pattern", deselect "Track Detector Pattern" and click on "User Pattern" to select user pattern. Then click on "Pattern" and "Load User Pattern" to select the OOB-01_COMRESET pattern from the SATA library.
3. Connect the PUT to the SATA receptacle
4. Enable the Data Output + (unlink and disable the Data Output – port) at V_{low} equal 0 V and V_{high} equal 2 V which will provide approximately 300 mV at the PUT.
5. On the BERTScope select the "Eye Diagram" view. Click on "Configure" and choose "Cursors" Select the "Single Cursor" and set it at 100 mV in the center of the eye. Stop the Eye Diagram from running. Click on "Configure" and "Cursors" again and choose the cursor to be the "Sampling Point"
6. Select "View" then "Editor" and "File" and click on "Capture by Length". Enter the capture length "11,255" words when prompted. Wait until data has been collected. Scroll down to see the COMINIT/COMRESET and COMWAKE burst of the PUT response. Count the average number of UIs of respectively the COMINIT/COMRESET and the COMVAKE gaps. The BERTScope Editor conveniently groups the data into 32 bits. 5 groups therefore correspond to 160 UI and 15 groups correspond to 480 UI. It is easiest to view the additional number of UIs when using binary representation, which can be selected in the "Edit" menu.
7. Repeat steps 6 through 8 above but with the threshold set to -100 mV.
8. Calculate the average of the gap lengths measured at +100 mV and -100 mV and multiply with the normalized UI namely 0.675106 ns (which takes into account that the average of the burst lengths measured at +100 mV and -100 mV is 158 UI) to get the gap lengths of the PUT in ns for the OOB-04 and OOB-05 measurements

Observable Results: The pass/fail criteria are:

OOB-04:

- COMINIT/COMRESET Transmit Gap Length measured to be between 310.4 ns and 329.6 ns

OOB-05:

- COMVAKE Transmit Gap Length measured to be between 103.5 ns and 109.9 ns

Test Title: OOB-06: COMWAKE Gap Detection Windows

Purpose: Verify that the Product Under Test, PUT, consistently enter speed negotiation for COMWAKE gap values between 155 UI and 165 UI and does not enter speed negotiation for COMWAKE gap values of 45 and 266 UI during OOB signaling per section 7.2.2.7.6 and 7.2.21 of Serial ATA revision 2.6.

Last Modification: March 9, 2009

Discussion: This test requirement is only tested at the maximum data rates 1.5 Gb/s and 3.0 Gb/s for PUTs claiming to be capable of running. The BERTScope transmits the COMRESET/COMINT sequence of 6 COMRESET/COMINIT 160 UI bursts with 480 UI gaps followed by a 45,000 UI gap plus a sequence of 6 COMWAKE 160 UI bursts with 160 UI gaps followed by a 130,000 UI gap and captures the 2 ms response for analysis according to sections 7.4.11 of the Serial ATA revision 2.6.

Resource requirements and setup for OOB are shown in Appendix E.

Test Procedure:

1. On BERTScope select "View" then "Generator" set the "Synthesizer" to 1.5 GHz and click on the "Clock Output" icon to enable these at full rate (divide by 1),
2. Click on "Pattern", deselect "Track Detector Pattern" and click on "User Pattern" to select user pattern. Then click on "Pattern" and "Load User Pattern" to select the OOB-06_45Gap_COMVAKE pattern from the SATA library.
3. Connect the PUT to the SATA receptacle
4. Enable the Data Output + (unlink and disable the Data Output – port) at V_{low} equal 0 V and V_{high} equal 2 V which will provide approximately 300 mV at the PUT.
5. On the BERTScope, select "View" then "Editor" and "File" and click on "Capture by Length". Enter the capture length "11,255" words when prompted. Wait until data has been collected. Scroll down to see if the PUT entered speed negotiation. Speed negotiation comes after the returned COMVAKE signaling and looks like a series of ALIGN symbols starting at the highest supported speed and shifting down every 54.6 us until the lowest speed is reaches if the PUT is a device. The hex representation of the repeated ALIGN symbols in the capture will be one of the following eight depending on the bit offset (1 out of 4 possible) and the disparity (1 out of 2 possible): 3E9555549C, 7D2AAAA938, FA55555270, 1F4AAAAA4E, C155555763, 82AAAAAEC7, 0555555D8F or E0AAAAABB1. Speed negotiation from a host comes after the returned COMVAKE signaling and looks like a series of D10.2 (0101010101 in binary or aaaaa or 5555 in hex) at the lowest speed if the PUT is a host.
6. Repeat above using each of the following pattern and associated capture length

Pattern	Capture Length
OOB06_45Gap_COMVAKE	**11,255 words**
OOB06_155Gap_COMVAKE	**45,185 words**
OOB06_165Gap_COMVAKE	**2,825 words**
OOB06_266Gap_COMVAKE	**22,585 words**

Observable Results: The pass/fail criteria are:

OOB-06a:
- The PUT did not enter speed negotiation in response to the OOB06a_COMVAKE_45 pattern which has a COMVAKE gap of 45 UI.

OOB-06b:
- The PUT did enter speed negotiation in response to the OOB06a_COMVAKE_155 pattern which has a COMVAKE gap of 155 UI.

OOB-06c:
- The PUT did enter speed negotiation in response to the OOB06a_COMVAKE_165 pattern which has a COMVAKE gap of 165 UI.

OOB-06d:
- The PUT did not enter speed negotiation in response to the OOB06a_COMVAKE_266 pattern which has a COMVAKE gap of 266 UI.

Test Title: OOB-07: COMINIT Gap Detection Windows

Purpose: Verify that the Product Under Test, PUT consistently responds to each COMINIT/COMRESET having gap windows between 459 UI and 501 UI and does not respond to COMINIT/COMRESET having gap windows of 259 UI and 791 UI during OOB signaling per section 7.2.2.7.7 and 7.2.21 of Serial ATA revision 2.6.

Last Modification: March 9, 2009

Discussion: This test requirement is only tested at the maximum data rates 1.5 Gb/s and 3.0 Gb/s for PUTs claiming to be capable of running. The BERTScope transmits the COMRESET/COMINT sequence of 6 COMRESET/COMINIT 160 UI bursts with 480 UI gaps followed by a 45,000 UI gap and captures the 2 ms response for analysis according to sections 7.4.11 of the Serial ATA revision 2.6.

Resource requirements and setup for OOB are shown in Appendix E.

Test Procedure:

1. On BERTScope select "View" then "Generator" set the "Synthesizer" to 1.5 GHz and click on the "Clock Output" icon to enable these at full rate (divide by 1),
2. Click on "Pattern", deselect "Track Detector Pattern" and click on "User Pattern". Then click on "Pattern" and "Load User Pattern" to select the OOB-07_259Gap_COMRESET_COMINIT pattern from the SATA library.
3. Connect the PUT to the SATA receptacle
4. Enable the Data Output + (unlink and disable the Data Output – port) at V_{low} equal 0 V and V_{high} equal 2 V which will provide approximately 300 mV at the PUT.
5. On the BERTScope, select "View" then "Editor" and "File" and click on "Capture by Length". Enter the capture length "47,255" words when prompted. Wait until data has been collected. Scroll down to see if the PUT repeatable responded with a correct COMINIT (if the PUT is a device) or COMWAKE (if the PUT is a host). COMINIT is a sequence of six 160 bit bursts with five 480 UI gaps. COMWAKE is a sequence of six 160 bit bursts with five 160 UI gaps.
6. Repeat above using each of the following pattern and associated capture length

Pattern	Capture Length
OOB07_259Gap_COMRESET_COMINIT	**47,255 words**
OOB07_459Gap_COMRESET_COMINIT	**48,255 words**
OOB07_501Gap_COMRESET_COMINIT	**48,465 words**
OOB07_791Gap_COMRESET_COMINIT	**49,915 words**

Observable Results: The pass/fail criteria are:

OOB-07a:

- The PUT did not respond to each COMINIT/COMRESET in the OOB07a_COMINIT_259 pattern which has a COMINIT/COMRESET gap of 259 UI.

OOB-07b:

- The PUT did respond to each COMINIT/COMRESET in the OOB07b_COMINIT_459 pattern which has a COMINIT/COMRESET gap of 459 UI.

OOB-07c:

- The PUT did respond to each COMINIT/COMRESET in the OOB07c_COMINIT_501 pattern which has a COMINIT/COMRESET gap of 501 UI.

OOB-07d:

- The PUT did not respond to each COMINIT/COMRESET in the OOB07d_COMINIT_791 pattern which has a COMINIT/COMRESET gap of 791 UI.

Appendix A: Initiation of PUT using BIST modes.

Purpose: The PUT is placed in one of two BIST modes, namely T+S+A or L and programmed with the desired test pattern as an initiation before the BERTScope measurements.

References:
1. Serial ATA Revision_2.6, section 10.3.9 BIST Active
2. U-Link Operating Help Files

Resource Requirements:
- Stimulus Tool: Any device or system capable of :
  i. Generating SATA OOB, negotiate speed and bringing the PUT to a state where it can receive a BIST Activate FIS.
  ii. Generating the required BIST Activate FIS, T,S,A or L respectively.

Examples of Stimulus Tools:
- BERTScope 7500B
- Intel ICH7 based computer with U-Link DriveMaster 2006 software version 3.0.198e or later.
- SCT-BIST Drive
- Serial ATA Protocol Generator/Analyzer
  a. JDSU Xgig

Last Modification: October 30, 2008

Discussion: The BERTScope acts as a monitoring tool fully capable of verifying the patterns transmitted by the PUT and can also generate SATA OOB, negotiate speed and bring the PUT to a state where it can register and receive a BIST Activate FIS in according to section 10.3.9 of the Serial ATA revision 2.5. When the BERTScope is used then there is no need for the SATA Tee as there will not be any disconnects.

The advantage of using a ULink BIST Initiation tool is that the combination of BERTScope and ULink provides a complete Digital and PHY/TSG/OOB and RSG test solution.

Test Setup: Stimulus Tool with an iSATA cable.

Test Procedure:
1. Connect PUT to the Stimulus Tool using the SATA cable.
2. Make sure that the Stimulus Tool is turned on and ready.
3. Allow the PUT to power up and go through OOB.
4. Initiate speed negotiation using the Stimulus Tool if change of speed is required.
5. Generate a BIST Active FIS with the appropriate bits set for either BIST T, A, S, including the pattern words or BIST L (preferred) as required using the Stimulus Tool.

10.3.9 BIST Activate - Bidirectional

0	Reserved (0)								Pattern Definition								R	R	R	R	PM Port				FIS Type (58h)							
									T	A	S	L	F	P	R	V															
1	Data1 [31:24]								Data1 [23:16]								Data1 [15:8]								Data1 [7:0]							
2	Data2 [31:24]								Data2 [23:16]								Data2 [15:8]								Data2 [7:0]							

Figure 197 – BIST Activate - Bidirectional

Field Definitions

FIS Type - Set to a value of 58h. Defines the rest of the FIS fields.

PM Port – When an endpoint device is attached via a Port Multiplier, specifies the device port address that the FIS should be delivered to or is received from. This field is set by the host for Host to Device transmission and this field is set by the Port Multiplier for Device to Host transmission. Endpoint devices shall set this field to 0h for Device to Host transmissions.

R - Reserved – shall be cleared to zero.

Pattern Definition

F – Far End Analog (AFE) Loopback (Optional)

L - Far End Retimed Loopback* Transmitter shall insert additional $ALIGN_P$ primitives

T - Far end transmit only mode

A - $ALIGN_P$ Bypass (Do not Transmit $ALIGN_P$ primitives) (valid only in combination with T Bit)

S - Bypass Scrambling (valid only in combination with T Bit)

P - Primitive bit. (valid only in combination with the T Bit) (Optional)

V - Vendor Specific Test Mode. Causes all other bits to be ignored

Data1 – Dword #1 of data information used to determine what pattern is transmitted as a result of the BIST Activate FIS. Applicable only when the T bit is set to one.

Data2 - Dword #2 of data information used to determine what pattern is transmitted as a result of the BIST Activate FIS. Applicable only when the T bit is set to one.

Example Using the U-Link Stimulus Tool:

1. Start the U-Link program
2. Click “Power Up” and observe the power supply spin up. Leave it on.
3. Click “CtlSATA”
4. Click COMRESET and observe that COMRESET was received on the log on the right side of the DriveMaster window.
5. Select the appropriate data rate “1” or “2” and observe that the “RDSTATUS” displays “00000113” or “00000123” for 1.5 Gb/s and 3 Gb/s respectively.
6. Select the appropriate “BIST mode T, S, A” for PHY and TSG Testing or “BIST mode L” for RTL Testing
7. When initiating PHY or TSG tests; select the desired pattern from the list.
8. Click “BIST” and observe that “BIST FIS SUCEEDED” is displayed in the lower left corner of the SATA Control Panel.
9. PUT should now be ready for test.

Possible Issues: Some PUTs may require sequences of ALIGN words before the desired pattern. This can be accomplished by using the pattern sequencing on the BERTScope having the B pattern be ALIGNs, which is then run once by a click on “Page Switch” followed by the A pattern, i.e. the desirable test pattern. AB patterns are pre-stored on the BERTScope for this purpose.

If the PUT lacks support of physical disconnect then a pair of couplers or power dividers are needed to be able to communicate with the PUT using the U-Link software on the computer and the BERTScope without physical disconnect.

Appendix B1: Calibration of Test Setup Differential Skew.

Purpose: Calibration of the skew between the Data + and Data - paths can improve the accuracy of the differential skew test in TSG-03.

Last Modification: January 5, 2009

Discussion: The skew between the Data + and Data - matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths can directly increase or decrease the measured differential skew of the PUT. This calibration removes the effect of these skews from the test. The calibration reference plane is the SMA interface where the SATA receptacle connects to the test setup.

Resource Requirements and Calibration Setup as shown in Appendix E: Except the BERTScope clock output is connected to the BERTScope clock input using the short SMA Male to SMA Male Cable. Initially connect the BERTScope Data Output + port via the short matched pair of SMA Male to Male Cables to the DUT Input + side of the SATA Tee in place of the SATA receptacle (connect to the short matched cables that connect to the CR 12500A Data Input + port if the SATA Tee is not used). Terminate the SATA Tee (or CR 12500A) Data Input - port with a 50 ohms termination. Disconnect the long matched cable that connects to the CR 12500A Data Output – and BERTScope Data Input – ports and terminate the CR 12500A Data Output - and the BERTScope Data Input - ports with the 50 ohms terminations. The BERTScope Data Output + port is now single ended connected via all the plus side cables and CR to the BERTScope Data Input + port.

Calibration Procedure:

1. Use the MFTP pattern, but generated by the pattern generator of the BERTScope Data Output + port. The MFTP pattern is pre-loaded on the BERTScope in "View", then "Generator", click on "Pattern", "User Pattern", "Load User File" then "SATA II" to select a pattern then click "Enable Outputs".
2. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" choose "CleanEye" from the "Eye Setup" menu and click on "Auto Center". Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Zoom in on the right most crossing by clicking on it and dragging it to the center of the display.
3. Click on "Eye Setup" on the BERTScope then "Cursors" and select "Time Cursors". Place one cursor at the mid point of the rising edge. Place the second cursor near by and zoom in on the mid point by changing the time and/or voltage scale. It is desirable to allow the time scale to show a full 20 ps to either side of the mid point cursor.
4. Move the cable from the BERTScope Data Output + port to the DUT Input – side of the SATA Tee (or if no SATA Tee is used; connect to the short matched of SMA Male to Male Cables that is associated with and connects to the CR 12500A Data Input – port). Terminate the SATA Tee (or CR 12500A) Data Input + port with the 50 ohms termination. Disconnect the long matched cable at the CR 12500A Data Output + port and connect this cable to the CR 12500A Data Output – port. Terminate the CR 12500A Data Output + port with 50 ohms. Leave the BERTScope Data Input - port terminated with 50 ohms. The BERTScope Data Output + port is now single ended connected via all the minus side short matched cable and CR to the BERTScope Data Input + port using the long matched cable associated with the BERTScope Data Input + port. This eliminates all generator, long matched cable and detector elements from the calibration as they are used for both measurements.
5. Place the second cursor at the mid point of the rising edge. The delta between the first and second cursor is the skew between the Data + and Data - matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths. All calibration screen shots need to be saved by clicking on "Print" and select "Print to file" then create a unique file name for each calibration data including the equipment serial number.

Observable Results: Record the calibrated differential skew for this value and the skew of the SATA receptacle test report to be subtracted from the measured differential skew in TSG-03.

Appendix B2: Calibration of Test Setup AC Common Mode.

Purpose: Calibration of the AC Common Mode insertion loss for TSG-04 measurements.

Last Modification: October 14, 2009

Discussion: The ratio of a 100 mV reference to the measured signal on the BERTScope is the inverse of the insertion loss. The measured data are then scaled with this factor to obtain the actual values. This calibration removes the effect of AC common mode insertion loss from the test. The reference plane for the calibrations is the SMA interface where the SATA receptacle connects to the test setup.

Resource Requirements and Calibration Setup as shown in Appendix E: Except the BERTScope clock output is connected to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the BERTScope Data Output + and Data Output - ports to the DUT Input ports of the SATA Tee (or to the short matched pair of SMA Male to Male Cables that connects to the CR 12500A Data Input ports if the SATA Tee is not used). Connect the Data Output + and - ports of the CR 12500A to the symmetrical input ports of the power combiner using the matched pair of cables. Connect the output of the power combiner to the low pass filter and connect the other end of the low pass filter to the Data Input + port on the BERTScope. Terminate the Data Input – port on the BERTScope with the 50 ohms termination.

Calibration Procedure:

1. The common mode insertion loss can be calibrated by simply applying a MFTP pattern from the BERTScope Data Outputs with 100 mV of common mode sinusoidal interference turned on to test setup; namely through the matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths ways, power combiner and low pass filter. The ratio of the 100 mV to the measured calibration signal on the BERTScope is the inverse of the insertion loss. The measured data are then scaled with this factor to obtain the actual values. All calibration screen shots need to be saved. This is done by clicking on "Print" and select "Print to file" then create a unique file name for each calibration data including the serial number of the equipment.

Observable Results: Record the ratio of the 100 mV reference to the measured signal. Measured data are then scaled with this factor to obtain the actual values in TSG-04.

Appendix B3: Calibration of Test Setup De-embedding.

Purpose: Measurement of the test setup insertion loss for de-embedding to the reference plane at the SMA side of the SATA receptacle. This applies to all TSG measurements except TSG-04 which is a common mode test.

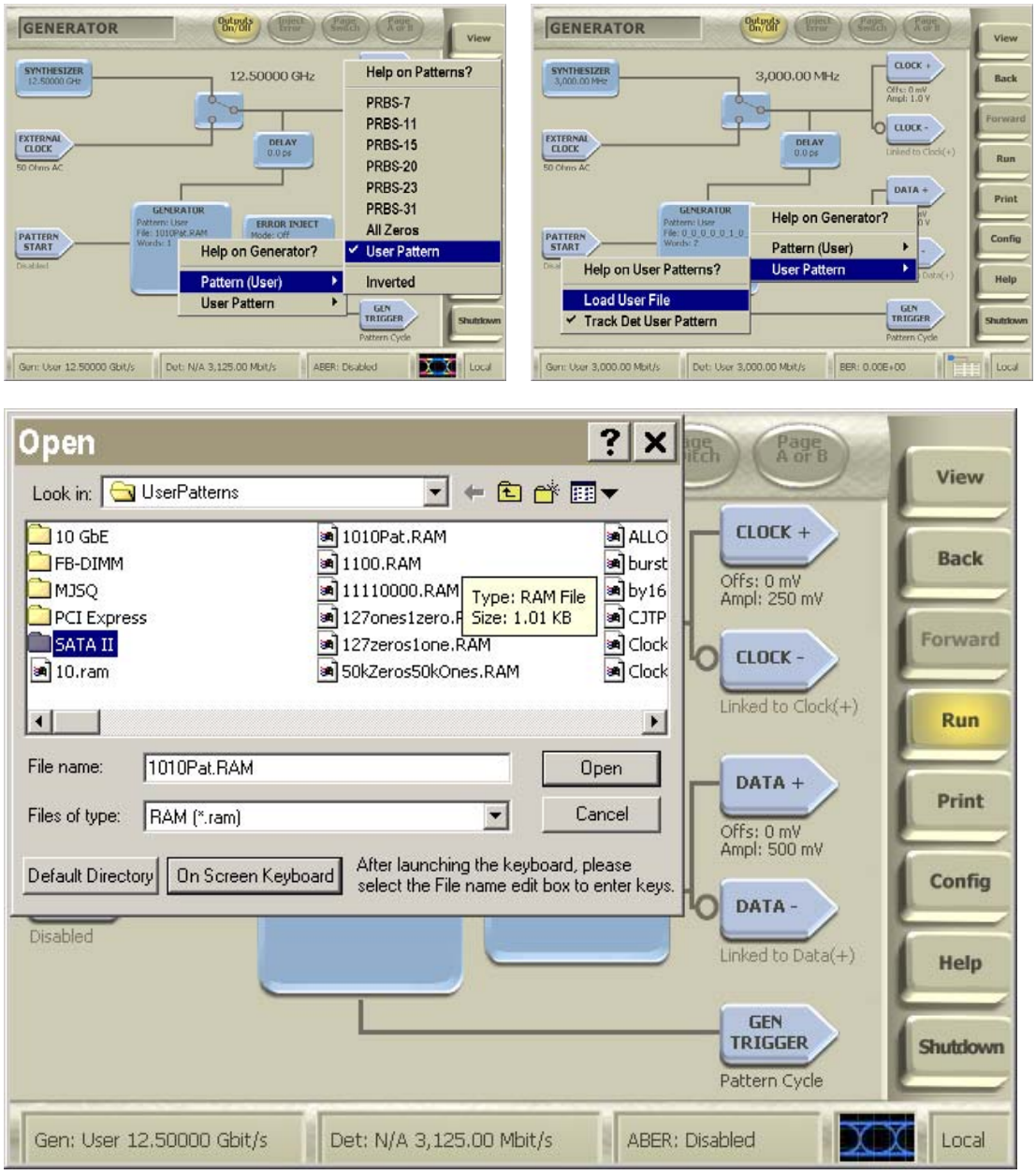
Last Modification: Mach 29, 2010

Discussion: The BERTScope is used to generate and capture the step response of the path through cables and other components to the BERTScope detector input. Fast Fourier Transformation (FFT) is applied to the step response, which is then subtracted from the FFT of a reference step response to get the insertion loss of the path. The BERTScope FIR Explorer software then calculates an FIR filter then compensates for the insertion loss. The reference plane for the calibrations is the SMA interface where the SATA receptacle connects to the test setup. This FIR filter is applied during TSG measurements, except TSG04, which is a common mode test.

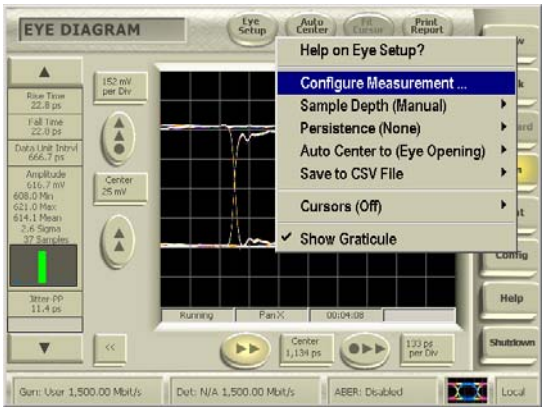
Resource Requirements and Calibration Setup as shown in Appendix E: Except the BERTScope clock output is connected to the BERTScope clock input using the short SMA Male to SMA Male Cable. Initially connect the BERTScope Data Outputs to the Data Inputs of the entire test setup; namely through the matched pair of short SMA Male to SMA Male cables connected via a pair of 50 ohms SMA female-to-female adapters to the reference plane where the SATA receptacle connects. Later the short matched pair of Data Output cables will be connected directly to the BERTScope Data Inputs for a reference measurement.

Calibration Procedure:

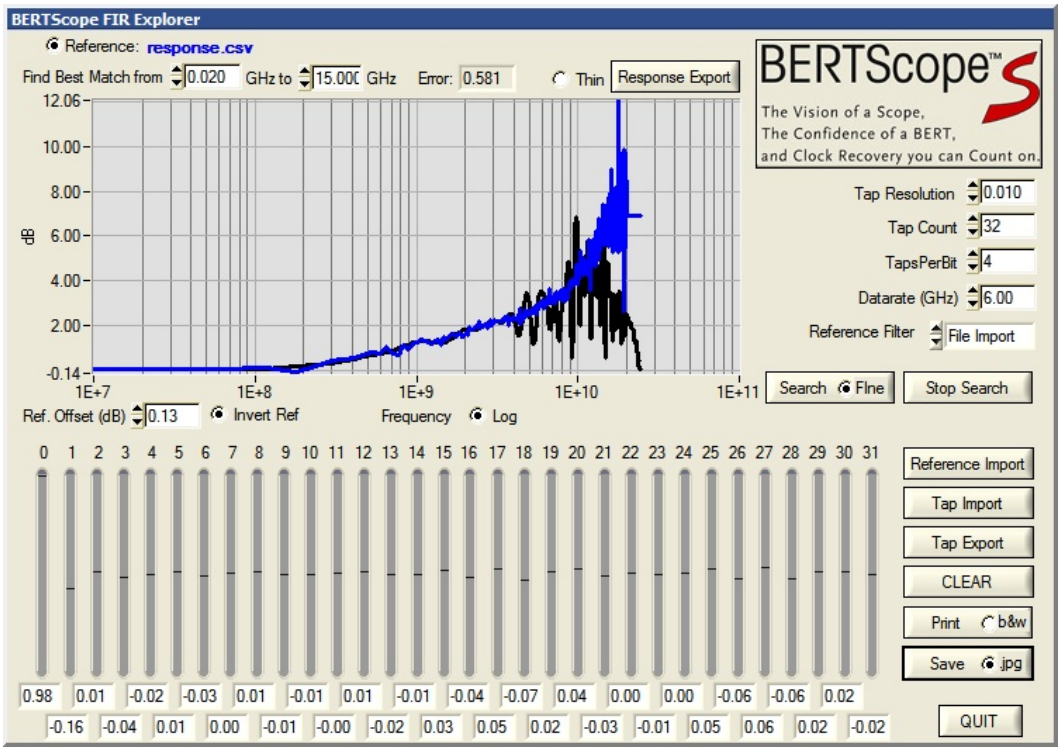
1. Set the data rate to 1.5 Gb/s by clicking on "Synthesizer" and set the Clock frequency to 1.5 Gbps.
2. Load the 32-zeros-64ones-32-zeros pattern in the generator and detector pattern memories. The patterns are pre-loaded on the BERTScope in "View", then "Generator", click on "Pattern", "User Pattern", "Load User File" then "SATA II" to select a pattern.



3. Enable the clock and data outputs by clicking on "Enable Outputs".
4. Click on "Eye Setup" and select "CleanEye" as the "Eye Operating Mode". Capture and save the Single-Value Waveform by stopping the "Run", clicking on " Eye Setup" and "Save to CSV" then select "Single-Value Waveform" with the following parameters; Pattern Length = 128 bits, number of samples per bit = 40, Y-axis.



5. Repeat Step 4 with the short pair of matched cables connected directly from the BERTScope Data Outputs to the BERTScope Data Input ports (no SATA Tee or Clock Recovery). This will be the reference single-value waveform. Remember to choose a file name different from the file name of the measurement waveform.
6. Open the "Insertion Loss Calculator.mcd" script in MatCad and insert the names of the reference (before) and measurement (after) waveform files using the 1 Gb/s measurement rate and 40 samples per UI.
7. Save the MatCad output file and open it as the reference file in BERTScope Explorer. Set the start and stop frequencies in BERTScope Explorer to respectively 20 MHz and 2.5 times the desired SATA data rate, i.e. 15 GHz for 6 Gb/s. Select "Inverted", 32 taps with 4 taps per UI and run the BERTScope Explorer application. Save the screen shot and the file using a unique file name for each calibration data including the data rate, date and serial number of the equipment.
8. Go to "Eye Setup", "FIR", "Configure" and enter the 32 tap values. Save as the insertion loss calibration FIR for the respective data rate.



9. Repeat Steps 7 and 8 for the other data rates.

Observable Results: The calibration and correction of test setup insertion loss is automatically applied when the appropriate data rare FIR filter is applied during the SATA tests. Correct filter can be selected for each data rate.

Appendix B4: Calibration of Test Setup OOB Amplitude.

Purpose: Calibration of the amplitudes used for OOB-01 tests.

Last Modification: March 29, 2010

Discussion: The amplitude of the OOB signal is measured and the best settings to achieve respectively 40 m V, 60 mV and 200 mV are found. The reference plane for the calibrations is the SMA interface where the SATA receptacle connects to the test setup.

Resource Requirements and Calibration Setup as shown in Appendix E: Except connect the BERTScope clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the BERTScope Data Outputs to the Data Inputs of the test setup; namely through the matched pair of short SMA Male to SMA Male cables connected via a pair of 50 ohms SMA female-to-female adapters to the reference plane where the SATA receptacle connects.

Calibration Procedure:

1. The OOB amplitude can be calibrated by simply applying the Align pattern from the BERTScope Data Outputs to the Data Inputs of the test setup; namely through the matched pair of short SMA Male to SMA Male cables connected via a pair of 50 ohms SMA female-to-female adapters to the reference plane where the SATA receptacle connects or to the DUT input side of the SATA Tee if a SATA Tee is used. Click on “Eye Setup” and select “CleanEye” as the “Eye Operating Mode”. Set the pattern length to “manual” and the value to “80”. Enable the FIR filter as calibrated in Appendix B3 for 1.5 Gb/s interface rate by clicking on “Eye Setup” then “Enable FIR”; “Configure FIR” and “Load Filter”. Measure and record the “Amplitude” All calibration screen shots need to be saved. This is done by clicking on “Print” and select “Print to file” then create a unique file name for each calibration data including the serial number of the equipment.

Observable Results: Record the setting needed to achieve the 40 mV, 60 mV and 250 mV OOB amplitudes needed for OOB-01 testing.

Appendix C: Jitter Transfer Function (JTF) calibration:

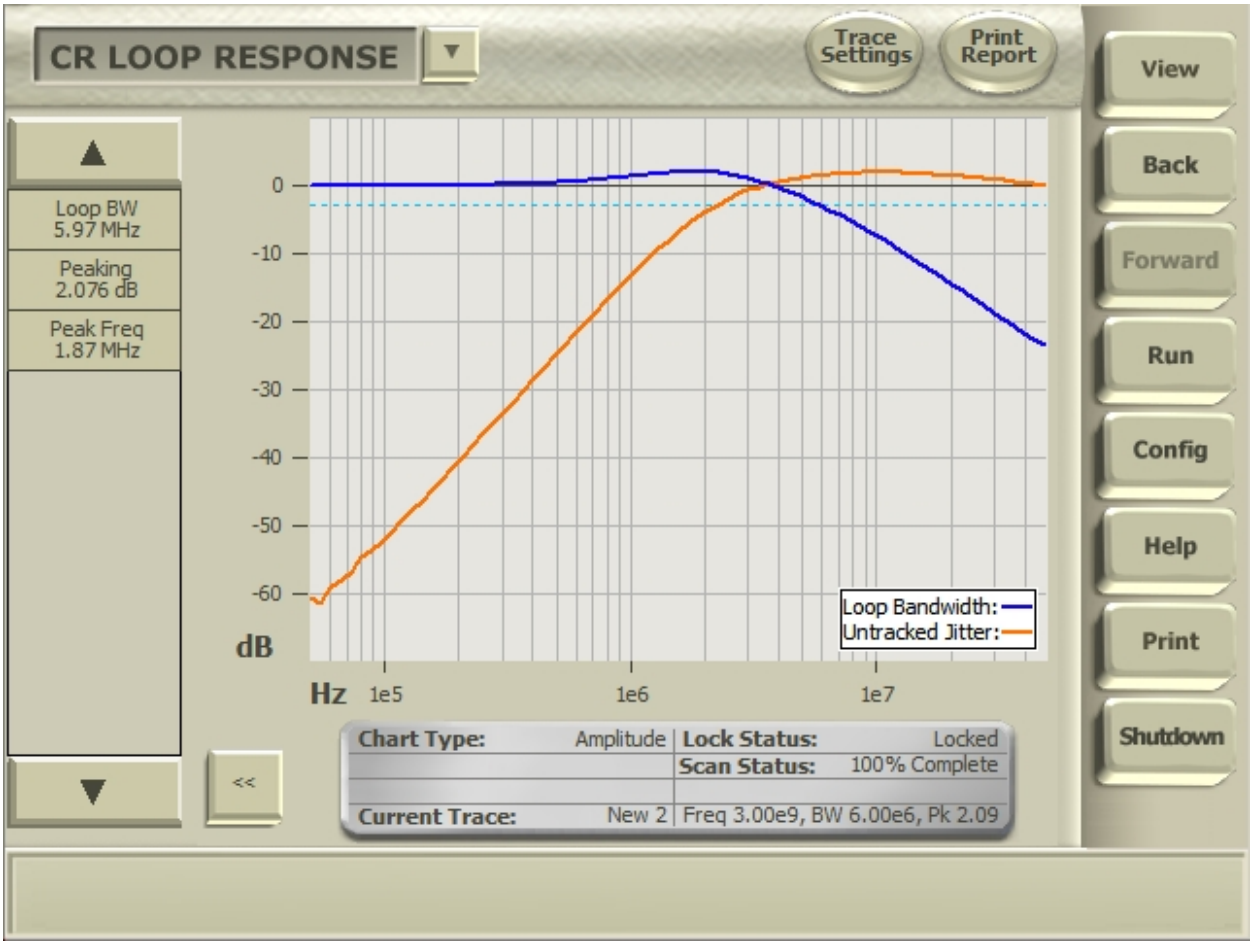
Description: The full JTF calibration require the injection of a reference signal, a MFTP pattern with jitter modulation from the BERTScope, and measurement of the jitter using the test setup detector, in this case the BERTScope detector with Clock Recovery (CR).

1. Set the CR to 2.09 dB peaking, this is the 0.707 damping factor required in Serial ATA.
2. Set the pattern generator to the MFTP pattern at 1 V amplitude. In "Generator" view turn on the SCC source, "Set it to Sinusoidal, Center Spread at 30 kHz and 3926 ppm.
3. Measure the ppm deviation, which is the difference between maximum deviation and minimum deviation in ppm of the SSC Waveform in the "SSC Waveform" view. Record this number as the reference ppm level.
4. Measure the received BUJ on the JitterMap View (or the DJ on the JitterPeak View if JitterMap is not available). .Adjust the CR 12500A closed loop bandwidth setting until the measured BUJ (or DJ) is between 4.9 ps and 5.5 ps (5.2 ps nominal). This provides the 72 dB +/-0.5 dB rejection at 30 kHz which is the most important parameter for the Jitter Transfer Function. (Approximate closed loop bandwidth setting for the CR is just below 6 MHz at 50% nominal edge density). The exact formula is as follows:

   Rejection (dB) = 10 LOG[(reference ppm level * 20.8 ns)/(3926 ppm * measured BUJ)]

   The 72 dB at 30 kHz sets a point on the steep slope of the JTF curve. The slope of the curve generally matches the roll-off of the spread spectrum clock spectrum and the reference clock phase noise. The combination of JTF and phase noise or SSC spectral density therefore approaches a constant value of measured jitter directly proportional to the location and accuracy of the 72 dB, 30 kHz point. That's a reason why this point is very important and set first.
5. Inject 50% UI (200 ps at 1.5 Gb/s, 100ps at 3 Gb/s) of sinusoidal jitter (SJ) at 50 MHz and measure the received BUJ on the JitterMap View (or the DJ on the JitterPeak View if JitterMap is not available). This BUJ (or DJ) value is the reference jitter level. It should be approximately equal to the injected SJ level.
6. Adjust the SJ frequency until 0.707 times the BUJ (or DJ) of the reference jitter level is achieved. Record the frequency as the 3 dB JTF bandwidth. This bandwidth is less critical, but must be within 2.1 MHz +/- 1 MHz.
7. Verify that the 3 dB JTF bandwidth is within 2.1 MHz +/-1 MHz.
8. Adjust the SJ frequency again to find the frequency, which yields the largest BUJ. This frequency will usually be above the 3 dB JTF bandwidth value and near the closed loop bandwidth value. Record the value of the largest measured BUJ as well as the associated SJ frequency.
9. Calculate the JTF Peaking as follows:
10. All digital edge based devices and ICs have peaking in the JTF response due to the delay in the digital circuitry, i.e. there is no phase information between edges in the data pattern, the pattern edge density and the fact that many phase detectors only detect on positive going edges. It is desirable to have as little peaking as possible and there are clock recovery options available to minimize the integrated area of peaking. Verify that the peaking is less than 3.5 dB.
11. Save the settings that meet above JTF as clock recovery standards "JTF-SATA1" and "JTF-SATA2" respectively for the 1.5 Gb/s and the 3.0 Gb/s calibrations. This is done by clicking on "View", "CR Control", "Standards" and "Create Standard"

Above full calibration should be done on the complete assembled SATA setup. A simpler measurement can be run more frequently on the CR itself. The CR12500A has a built in calibration and verification circuitry called "CR Trace", which can be activated from the BERTScope (or from a PC). Below please find an example of the CR Trace verification plot.


CR LOOP RESPONSE
Trace Settings
Print Report
View
Back
Forward
Run
Config
Help
Print
Shutdown
Loop BW
5.97 MHz
Peaking
2.076 dB
Peak Freq
1.87 MHz
0
-10
-20
-30
-40
-50
-60
dB
Hz
1e5
1e6
1e7
Loop Bandwidth:
Untracked Jitter:
<<
Chart Type: Amplitude
Lock Status: Locked
Scan Status: 100% Complete
Current Trace: New 2
Freq 3.00e9, BW 6.00e6, Pk 2.09

Appendix D: Validation of Lab Load Return Loss

Purpose: Prior to use of the BERTScope test setup, the Lab Load, for PHY and TSG compliance testing, the return loss must be verified to be better than required by the Serial ATA Revision 2.6 section 7.2.2.5.

References:

1. Serial ATA Revision 2.6

Resource Requirements:

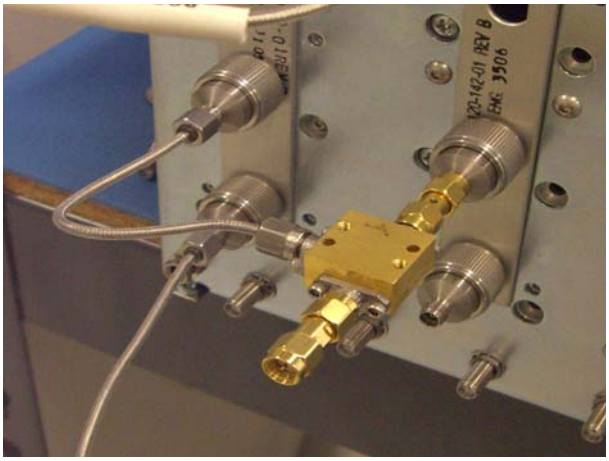
- Appendix E plus the following:
- Two short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- Two SMA Male to SMA Male Adapters, SUHNER 32SMA-50-0-1 or equivalent
- Two power combiners, Weinschel 1515 or equivalent
- Two 50 ohm terminations, SUHNER or equivalent
- Two short circuits, SUHNER or equivalent

Or

- A 8 GHz Vector Network Analyzer, R&S or equivalent with calibration kit

Last Modification: June 6, 2009

Test Setup: Connect the power combiner, SMA adapter and cable pairs to the BERTScope Clock Outputs and Data Input as shown in the photo.



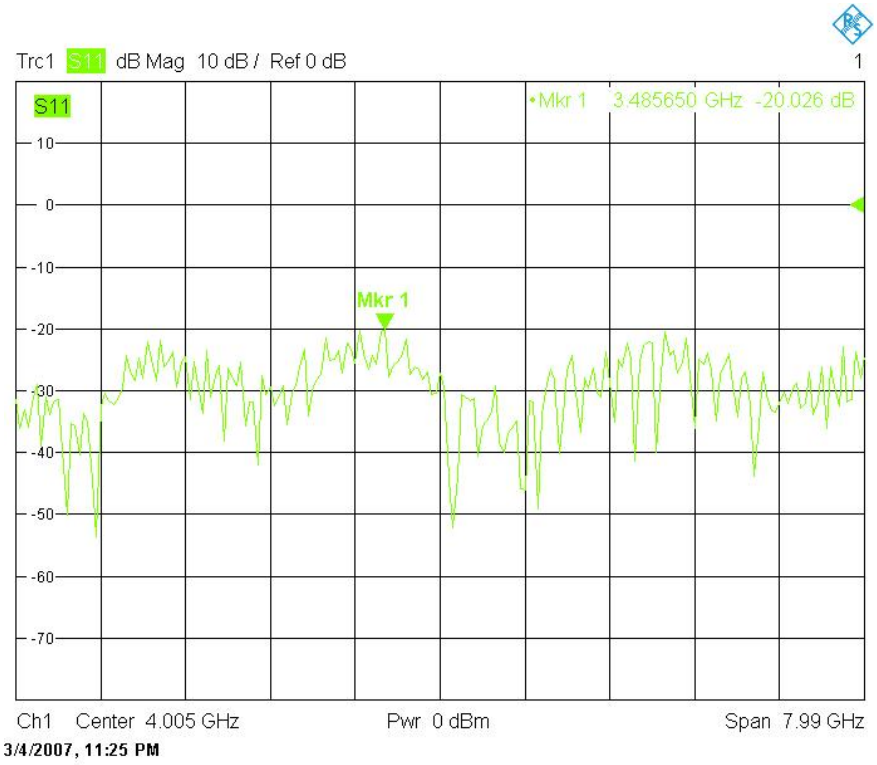
Test Procedure:

1. Power-on the SATA Tee and the Keithley switch of the BERTScope Serial ATA setup to be tested.
2. Send the 34-zeros-64-ones-34-zeros step response pattern at 1.5 Gb/s with Clock Outputs set to divide-by-32 and at 1 Volt nominal amplitude towards respectively the termination, short circuit and the port to be tested (obviously the one not used by the return loss power combiner circuitry) and capture the 128 bit long response in the "Eye Diagram" view using the "Clean Eye" export to csv in y-axis format at least 40 samples per bit resolution.
3. Open the MatCad script as per Appendix B4 to run the FFT on the captured data using the responses from the 50 ohm terminations and the short circuits to provide the 50 ohm and zero time reference points.
4. Repeat steps 1 through 3 with the BERTScope Data Input Port terminated in 50 ohms for single port measurements as needed.

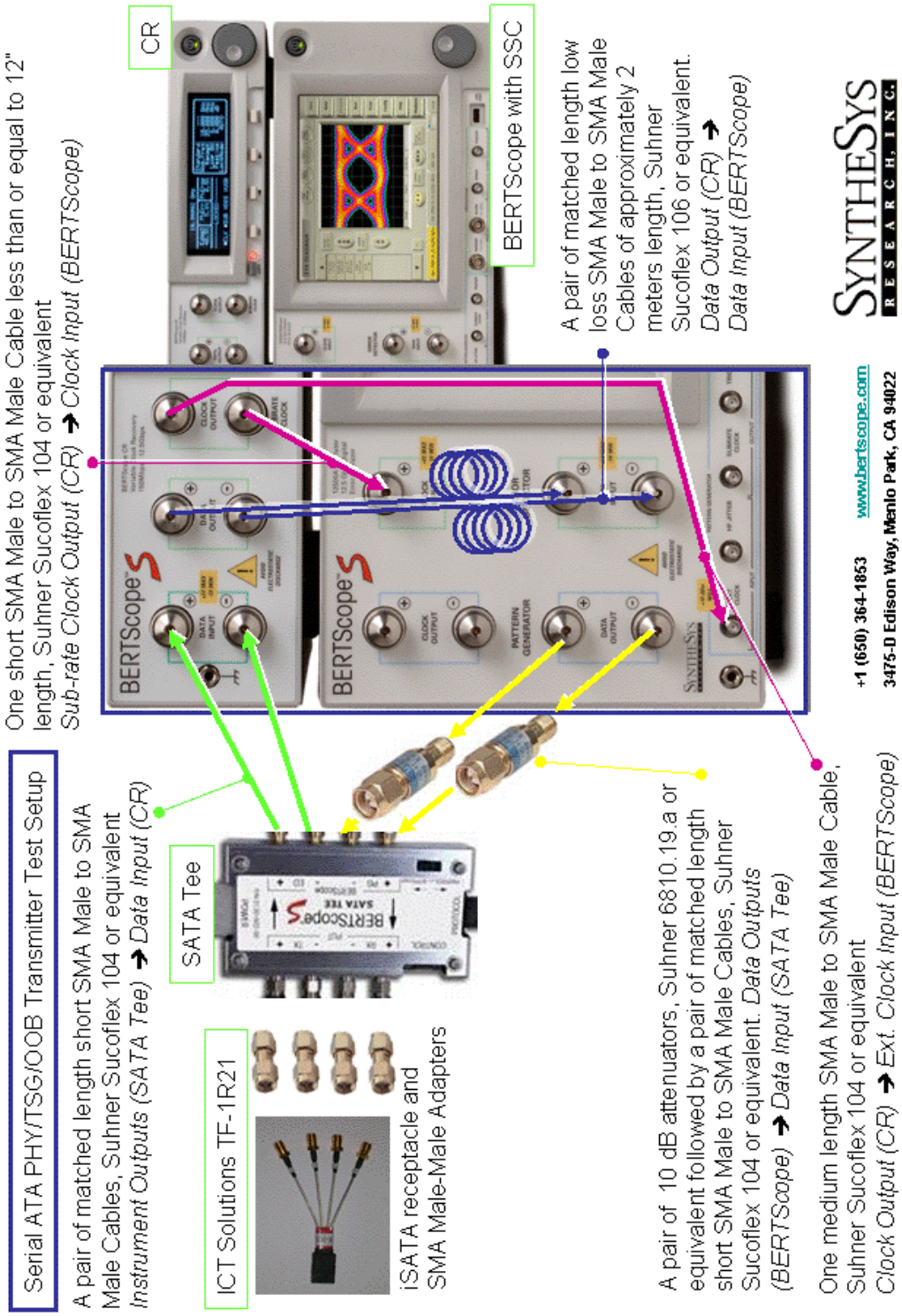
Observable Results: The pass/fail criteria are:

- The Return loss of each port must be better than specified in Serial ATA Revision 2.6 section 4.2.2.5 Laboratory Load; namely: The inputs of the Laboratory Load (from the back of the mated SATA

connector to the 50 ohm load within the HBWS) shall have an individual return loss greater than 20 dB over a bandwidth of 100 MHz to 5.0 GHz, and greater than 10 dB from 5 GHz to 8 GHz.



Appendix E: Serial ATA Interoperability Program Test Setup using BERTScope[1].



[1]Setup including cables and adaptors to have return loss per SATA specifications and be deskewed to within 1 ps.

Last Modification: January 5, 2009

Resource Requirements Summary for all PHY and TSG and OOB tests as covered by this MOI:

- One BERTScope "B" or "C" with software version 10.5 or later
- One BERTScope PatternVu software option
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8 or later
- One iSATA receptacle to SMA Female Adapter, Wilder SATA-TPA-R 600-1014-000 or ICT Solutions TF-1R21 or equivalent
- One BERTScope CR cables set, CR 12500ACBL, consisting of:
    i. One short SMA Male to SMA Male Cable less than or equal to 8" length, must be phase/ delay matched to the BERTScope setup and the 2 meter cable pair.
    ii. A pair of matched length short SMA Male to SMA Male Cables of about 1 meter length
    iii. A pair of matched length low loss SMA Male to SMA Male Cables of 2 meters length
- A second pair of matched length short SMA Male to SMA Male Cables of approximately 1 meter length, Suhner Sucoflex 104 or equivalent
- Three 50 ohms terminations, SUHNER 65SMA-50-0-1 or equivalent
- One pair of 10 dB SMA Male to SMA Female Attenuators, SUHNER 6810.19A or equivalent
- One pair of 6 dB SMA Male to SMA Female Attenuators for OOB tests, SUHNER 6806.19A or equivalent unless the A BERTScope SATA Tee and SMA Adapters are used.
- One passive power combiner, Weinschel 1515 or equivalent
- One first order low pass filter having a cutoff equal to the bitrate/2, namely 1.5 GHz, Pico Seconds Pulse Lab, 5915-110-1.5GHz or equivalent.
- One BIST initiation tool as per Appendix A such as above BERTScope "B" or "C"

To support non-disconnect PUTs the following is useful:

- BERTScope SATA Tee Test Fixture if needed for support of non-disconnect PUTs.

For Automation you may further want to have:

- Switch, Keithley S46TX0000000TTTTA
- Ethernet to GPIB interface for Keithley switch
- 7 Cables 6" each for switch: Astro lab Mini-bends 32081-2-29094C-6 or equivalent
- BERTScope Serial ATA Interop Test Suite software, revision 1.1

The calibrations of Skew, FIR, JTF and verification of return loss in Appendix B through D must be done after assembling the setup and before starting the testing.

PHY/TSG/OOB Test Setup as shown: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect a second cable from the CR 12500A clock output to the BERTScope Ext. Clock input to support the proprietary synchronized loopback mode. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of low loss cables. Connect both of the B+ and B- ports of SATA receptacle, these are the pins marked 6 and 5 respectively (via the SMA adapters and the SATA Tee if used) and the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports. Connect both of the A+ and A- ports of SATA receptacle, these are the pins marked 2 and 3 respectively (via the SMA adapters and the SATA Tee if used) 10 dB attenuators (and 6 dB attenuators if OOB testing without a SATA Tee) and the short matched pair of SMA Male to Male Cables to the respective BERTScope Data Output + and - ports. Above connections are for Device testing. For host testing simply rotate the SATA Receptacle 180 degrees thereby switching pin 2 with 6 and pin 3 with 5.

OOB Test Setup as shown: Except connect the BERTScope clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. One could connect B+ and B- ports of SATA receptacle directly to the BERTScope Data Inputs without the CR for the OOB tests, however for similarity to the other PHY and TSG tests connection via the CR is described. Above connections are for Device testing. For host testing simply rotate the SATA Receptacle 180 degrees thereby switching pin 2 with 6 and pin 3 with 5.